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The Development of a New Fibonacci Switched-Capacitor DC-DC Converter and its Analysis Method

by

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Abstract

DC-DC power converters are sorted into inductor-based and inductor-less converters according to whether they consist of magnetic components such as inductors or transformers. Switched capacitor (SC) DC-DC converters are one of the representative examples in the category of inductor-less converters. SC DC-DC converters can reduce EMC (electromagnetic compatibility) and EMI (electromagnetic interference) problems and minimize their size because they have no magnetic components. These characteristics fit in mobile products industries including wearable devices, smart cards, IoT and so on. Among them, this work focuses on energy harvesting systems.

Up to now, many different types of SC DC-DC converters have been proposed and modified. Taking symmetric Dickson topologies for example, their power efficiency and output ripple voltage improved but their circuit size became bigger than a normal Dickson topology. Cross-connected Fibonacci topologies have the same flaws. For these reasons, the goal of this research is to design a novel SC DC-DC converter for the energy harvesting systems.

In order to suggest a new SC DC-DC converter, this work starts from selecting an analysis way in Chapter 2. In this thesis, all SC DC-DC converter topologies in a steady state are analyzed by the four-terminal equivalent (FE) circuit model. The suitability of the FE model is verified through an analysis of the gain function of a trivial SC DC-DC converter.

In Chapter 3, we categorize SC DC-DC converter topologies as core or modified topologies by the number of their outermost mesh including input and output ports. These topologies are modeled by the FE model and simulated to measure their power efficiencies and output ripple voltages. Then, we compare the topologies according to the core topologies and their family group at different conversion ratios from 2 to 20.

In Chapters 4 and 5, we suggest two new SC DC-DC converter topologies that are named cross-connected Dickson topology and enhanced cross-connected Fibonacci topology. Each of the new topologies is based on the Dickson topology and Fibonacci topology, respectively. We analyze and simulate two proposed topologies. Then, the suggested topologies are compared with their family group, respectively. Moreover, the feasibility of two new topologies are verified by building them on a breadboard.

Chapter 6 summarize this work and discuss the future works.

Keywords: Switched Capacitor DC-DC Converter, Cross-connected Topology, Switched Capaticor Converter Topology Comparison, Energy Harvesting System.

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Chapter 1

Introduction

1.1 Switched Capacitor DC-DC Converter

DC-DC power converters are categorized according to whether or not they are designed with magnetic components. A power converter with magnetic components is called an inductor-based or transformer-isolated converter [1]. Typical examples are non-isolated topologies (e.g. buck, boost, buck-boost, etc.) and isolated topologies (e.g. flyback, half-forward, forward, resonant forward, etc.) [2]. Although the inductor-based converters have been utilized in many different products for decades, the magnetic components of them cause electromagnetic interference and electromagnetic compatibility problems [3–5]. Furthermore, they make the circuit size bulky. For this reason, it was demanded to design a power converter without magnetic components or an inductor-less converter. As a subgroup of inductor-less converters, switched capacitor (SC) DC-DC converters satisfy such the demand, because they consist of switches and capacitors without magnetic components.

In previous studies, the SC power converters have been developed as follows: H. Greinacher proposed the first idea of voltage multipliers with capacitors and diodes or SC converters in 1914 and then suggested a cascaded type of SC converters [6]. In 1932, J. D. Cockcroft and E. T. S. Walton suggested the Cockcroft-Walton multiplier and utilized it for their physic experiment [7, 8]. Modifying the Cockcroft-Walton multiplier, J. F. Dickson designed the Dickson charge pump in 1976 [9]. In 1989, F. Ueno et al. established a basis of SC converters' design and its control [10]. In 1995, O. C. Mark et al. suggested a series-parallel type of SC DC-DC converters [11]. Fibonacci topologies of SC DC-DC converters are proposed by F. Ueno et al [12,13].

Based on three core topologies (Dickson, series-parallel and Fibonacci), they have been modified to improve their performance by a myriad of researchers. As a modified topology of the series-parallel topology, a switched capacitor voltage multiplier (SCVM) topology was examined by Y.-H. Chang et al [14]. The SCVM topology is connecting more than two the series-parallel topologies in series. L. Salem and P. Mercier proposed a symmetric series-parallel topology by cascading the converters to generate multioutput [15]. To improve the power efficiency of the Dickson topology, the symmetric Dickson topologies were suggested by many works and studies [16–21]. In the symmetric structure, two Dickson converters are connected in parallel. In the study [22], an k $(= 2, 3, \ldots)$-Fibonacci topology was suggested by K. Eguchi et al. The k-Fibonacci topology improved the power efficiency of the normal Fibonacci topology with its multioutput. A symmetric Fibonacci topology was designed in the study [23].

As the above-mentioned topologies are step-up topologies of SC DC-DC converters, this thesis focuses on them.

1.2 Application of Switched Capacitor DC-DC Converter

Up to now, SC DC-DC converters have been utilized for various commercial products and industries. They have required relatively simple power conversion ratios such as 0.5 and 2 times the input voltage of the products. The converters have been used in programming voltage generators of non-volatile memories such as USB flash memories, EEPROM (electrically erasable programmable read-only memory) or SSD (solid-state drives) [24–29]. However, recent demands for the SC DC-DC converter increase in high tech-industries. As examples of applications in the industries, there are LED driver circuits [30–33], RFID related products [34–40], medical instruments [41–43], wearable devices [44–49], etc.

Among the industrial parts, this thesis targets the mobile products industry including IoT, wearable devices and so on. This is because the products can be operated by energy harvesting systems that is one of the eco-friendly technologies. The process of energy harvesting is to take energy from ambient sources such as thermal energy [50–54], kinetic energy [55–59], solar energy [60–62], etc. Then, that

energy is converted and is stored to transfer to mobile products that need it. The energy harvesting systems require an SC DC-DC converter with its high gain and power efficiency, because their input voltages are ultra-low [63–67]. The goal of this research is to suggest a novel SC DC-DC topology that can be used for the energy harvesting systems.

1.3 Previous Researches by Others and Emphases in This Work

An SC DC-DC converter suggested by Eguchi et al. has two input sources of the clean energy and battery [68, 69]. This way can provide stable input power, but the circuit size of the converter is bigger. Wang et al. proposed a split-merge Dickson topology [70, 71]. Although the output performance is improved, the split-merge converter is operated by multi-phase operation clock. This operation leads to a complex control. Modified Dickson topologies of SC DC-DC converters were proposed by Doms et al. and Yun et al. for thermoelectric generators [40,52,72]. The Dickson topologies transfer step-up voltages to their load during only half period of their operation period.

In this thesis, emphases in designing a new topology are summarized as follows:

- Reduction of circuit components
- Two-phase operation
- Improvement of power efficiency
- Continuous delivery of step-up voltage

1.4 Purpose and Contribution in This Work

In this thesis, we suggest two new SC DC-DC converter topologies for mobile products including energy harvesting systems. To propose new topologies, it is essential to establish an analysis and modeling way in order to design SC DC-DC converters. In Chapter 2, we select a modeling way through examining a trivial SC

DC-DC topology and distinguishing dominant parameters to affect output performances of SC DC-DC converters in a steady state. The model is called four-terminal equivalent (FE) circuit model [73–76].

Chapter 3 performs a comparative study with 6 SC DC-DC converter topologies. The topologies are categorized as core topologies and modified topologies according to the number of their outermost mesh including input and output ports. This comparative study can provide a selecting standard or evaluating criteria when future developers research or use one of the topologies.

In Chapter 4, we suggest two new modified topologies. Two topologies are based on the Dickson and Fibonacci topology, respectively. The suggestion of the first new topology is a processing of designing the new Fibonacci topology, or the second new topology. This is because the first proposed topology had a problem of its circuit size as increasing its conversion ratio if two topologies have the similar number of circuit components. Furthermore, there was a room for improving the step-up gain of the topology at specific conversion ratios. For these reasons, this work includes the design of two new topologies.

In Chapter 5, the new topologies are analyzed by the modeling way selected in Chapter 2. Then, we simulate and compare each topology with their own family topologies. Lastly, feasibilities of two new topologies are confirmed by building them on a breadboard.

Chapter 6 makes a conclusion of this work and discusses future studies.

Contributions of this work are condensed as follows:

- Establishment of the suitability of the FE model in analyzing SC DC-DC converter topologies in a steady state
- Proposal of topology-classification standard for SC DC-DC converter topologies as core or modified topologies
- Comparative study with 6 different SC DC-DC converter topologies to make a selecting and evaluation standard and to benefit future researchers
- Proposal of two new SC DC-DC converter topologies with the consideration of energy harvesting system
- Verification of workabilities of the suggested topologies

Chapter 2

Aanalysis of Switched Capacitor DC-DC Converter

SC DC-DC converters consist of switches and capacitors [77]. These switches are turned on and off according to their topologies and switching rules. This operation leads the SC DC-DC converters to have their instantaneous equivalent circuits. Based on these equivalent circuits, an analysis of the SC DC-DC converters is implemented.

2.1 Four-terminal Equivalent Circuit Model

In a steady state, the topologies of the SC DC-DC converters in this thesis are analyzed by using the four terminal equivalent circuit model (FE model) as shown in Figure2.1 [73–76, 78]. The four-terminal equivalent circuit model consists of the input and output voltage and current, the ideal transformer, the parameter of R_{SC} and the output load. The turn ratio (1: m) of the ideal transformer expresses the ideal conversion ratio of a targeted SC DC-DC converter. The value of R_{SC} is the parameter based on the consumed energy of on-resisters of switches in the SC DC-DC converter during one operation cycle. Therefore, R_{SC} is called the output impedance. In the FE model, the R_{SC} and R_L are the only components to consume the energy from the input and to have an impact on the output performance. The goal of the modeling using this model, therefore, is to derive R_{SC} of the target converter and to analyze the output performance based on its consumed energy.

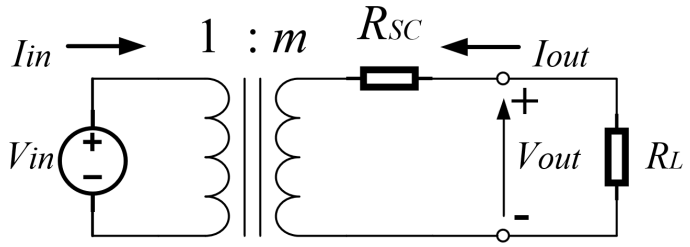


Figure 2.1: Four-terminal equivalent circuit model.

2.1.1 Trivial Topology Analysis

Figure 2.2 shows a trivial SC DC-DC converter with the conversion ratio of 1 to 1. The trivial SC DC-DC converters is operated by turning on and off the switch with on-resistor R_{on} in order to charge the capacitor of capacitance C and to transfer its charge to the output load R_L. In the switching period of T, the relation of the duty ratio and the period, DT, indicates the off-time of the switch.

The analysis of the trivial SC DC-DC converter in a steady state is based on its instantaneous equivalent circuits as shown in Figure 2.3. From Kirchhoff's current & voltage law (KCL & KVL) and the first-order differential equation of the RC circuits (the equivalent circuits), the capacitor voltage during State-1 can be calculated by:

$$V_{C,s\text{-}1}(t) = \left(V_{C,min} - \frac{R_L}{R_L + R_{on}} V_{in}\right) e^{-\frac{R_L R_{on}}{(R_L+R_{on})C}t} + \frac{R_L}{R_L + R_{on}} V_{in}, \tag{2.1}$$

where $V_{C,min}$ is the minimum voltage of the capacitor.

Using the same way in State-1, the capacitor voltage during State-2 is given by:

$$V_{C,s\text{-}2}(t) = V_{C,max} e^{-\frac{1}{R_L C}t}, \tag{2.2}$$

where $V_{C,max}$ is the maximum voltage of the capacitor.

According to the principle of capacitor amp-second balance or capacitor charge balance [2], the maximum and minimum capacitor voltage, $V_{C,max}$ and $V_{C,min}$, can be expressed by:

$$\begin{aligned} V_{C,max} &= V_{C,s\text{-}1}((1-D)T) = V_{in} \cdot \frac{R_L}{R_L + Ron} \cdot \frac{1 - e^{-\frac{(1-D)R_L R_{on} T}{(R_L+R_{on})C}}}{1 - e^{-\left\{\frac{(1-D)R_L R_{on} T}{(R_L+R_{on})C} + \frac{DT}{R_L C}\right\}}}, \\ V_{C,min} &= V_{C,s\text{-}2}(DT) = V_{C,max} \cdot e^{-\frac{DT}{R_L C}}. \end{aligned} \tag{2.3}$$

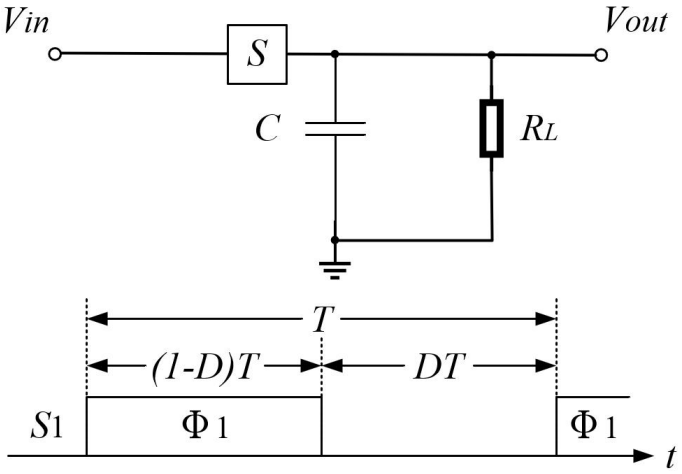


Figure 2.2: Trivial SC DC-DC converter with the conversion ratio of 1 to 1.

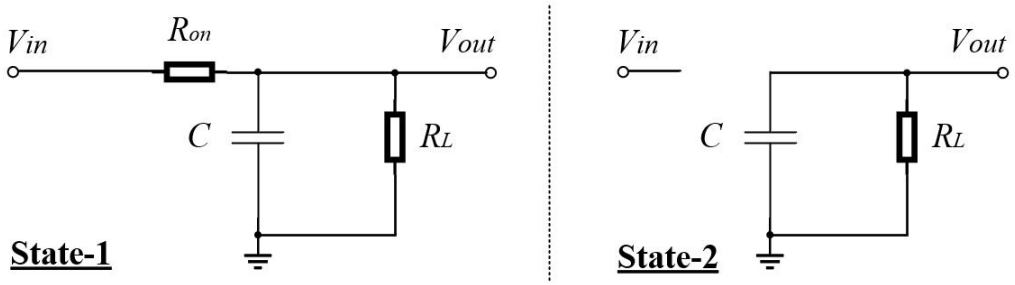


Figure 2.3: Instantaneous equivalent circuits of the simple SC DC-DC converter.

For one operating cycle, the average output voltage $\langle V_{out} \rangle$ is the same to that of the capacitor $\langle V_C \rangle$. The relation of them is given by:

$$\langle V_{out} \rangle = \langle V_C \rangle = \frac{\int_0^{(1-D)T} V_{C,s\text{-}1}(t)dt + \int_0^{DT} V_{C,s\text{-}2}(t)\,dt}{T}. \tag{2.4}$$

From 2.4, the relation of the input and output voltage and the gain function $G(R_{on}, R_L, C, T, D)$ is obtained by:

$$\begin{aligned} \langle V_{out} \rangle =& G(\gamma)\,\langle V_{in} \rangle\,, \\ G(\gamma) =& \frac{R_L R_{on}}{R_L + R_{on}} \left[\frac{R_L R_{on}}{R_L + R_{on}} C \left\{ \frac{(1-\alpha)\,\beta}{1-\alpha\beta} - 1 \right\} + (1-D)\,T + \right. \\ & \left. R_L C \frac{(1-\alpha)\,(1-\beta)}{1-\alpha\beta} \right] \frac{1}{T}, \end{aligned} \tag{2.5}$$

where $\alpha = e^{-\frac{(R_L+R_{on})(1-D)T}{R_L R_{on} C}}$, $\beta = e^{-\frac{DT}{R_L C}}$ and $\gamma = R_{on}, R_L, C, T, D$.

Table 2.1: Default setting of the trivial SC DC-DC converter.

Parameter	Value	Variable
R_L	1kΩ	20Ω∼5kΩ
R_{on}	1Ω	10Ω∼1kΩ
C	10μF	1μF∼ 1000μF
D	0.5	0.1∼0.9
$T(f)$	1μs(1MHz)	0.1μs∼1s(1Hz∼10MHz)

2.1.2 Dominant Parameters

The trivial topology analysis indicates a characteristic of SC DC-DC converters that their output performances are affected by the parameters: D, T, C, R_L, R_{on}. In the gain function $G(\gamma)$, the different coefficients of the parameters lead to the idea that there exist the dominant ones among the parameters to impact the power efficiency or output voltage of the SC DC-DC converters.

Figure 2.4 shows the extent to which each parameter has an effect on the gain of the trivial SC DC-DC converter. The default setting of the parameters is shown in Table 2.1, whereby the only targeted parameter is varied. The gain variation with the load value and on-resistor in Figure 2.4(a) and Figure 2.4(b) is approximately 0.9∼1 and 0.3∼1, respectively. The gain variation with the capacitance and duty ratio is neglectable as shown in Figure 2.4(c) and Figure 2.4(d) as the varying range are from 0.99792 to 0.998004 and from 0.9989 to 0.9901, respectively. As long as the frequency is over 1kHz, the gain keeps above 0.9 as depicted in Figure 2.4(e). Consequently, it can be confirmed that the dominant parameters in a steady state are R_{on} and R_L.

2.1.3 FE Model

A modeling of a targeted SC DC-DC converter in a steady state based on the FE model is processed by three steps. (1) Derive the conversion ratio m by analyzing the instantaneous equivalent circuits of the targeted converter. (2) Calculate consumed energy by on resistors of switches in the converter during one operating cycle, by which R_{SC} is given. (3) Yield the maximum power efficiency and output voltage of the converter.

The trivial SC converter in Figure 2.2 can be modeled by using the FE model. First of all, according to the principle of capacitor amp-second balance, the relation of the electric charge amount of the capacitor for each operating cycle, $\Delta q_{T_i} (i = 1, 2)$, is given by:

$$\sum_{i=1}^{2} \Delta q_{T_i} = 0. \tag{2.6}$$

By setting the duty ratio D to 50%, T can be written as:

$$T = \sum_{i=1}^{2} T_i \quad \text{and} \quad T_1 = T_2 = \frac{T}{2}, \tag{2.7}$$

where $T_1 = (1 - D)T$ and $T_2 = DT$.

From Figure 2.3, the relations of the electric charge amount in the input, output and capacitor, $\Delta q_{T_i,V_{in}}$, $\Delta q_{T_i,V_{out}}$ and Δq_{T_i}, are given by:

$$\begin{aligned} &\text{State-1}: \quad \Delta q_{T_1,V_{in}} = \Delta q_{T_1} + \Delta q_{T_1,V_{out}}, \\ &\text{State-2}: \quad \Delta q_{T_2,V_{in}} = 0, \quad \Delta q_{T_2,V_{out}} = -\Delta q_{T_2}. \end{aligned} \tag{2.8}$$

According to the definition of electric current, the average input and output current in one operating cycle, $\langle I_{in} \rangle$ and $\langle I_{out} \rangle$, can be calculated by:

$$\begin{aligned} \langle I_{in} \rangle &= \frac{1}{T} \left(\sum_{i=1}^{2} \Delta q_{T_i,V_{in}} \right) = \frac{\Delta q_{V_{in}}}{T} \quad \text{and} \\ \langle I_{out} \rangle &= \frac{1}{T} \left(\sum_{i=1}^{2} \Delta q_{T_i,V_{out}} \right) = \frac{\Delta q_{V_{out}}}{T}. \end{aligned} \tag{2.9}$$

Substitution of Eq. 2.6 into Eq. 2.9 for the relation of the input and output current yields

$$\langle I_{in} \rangle = - \langle I_{out} \rangle , \tag{2.10}$$

where $\Delta q_{V_{in}} = -\Delta q_{V_{out}}$. From Eq. 2.10, the conversion ratio $m_{trivial}$ is given by:

$$m_{trivial} = 1. \tag{2.11}$$

Next, by using Eqs. 2.6 - 2.8, the consumed energy of the on-resistor can be calculated by:

$$\begin{aligned} &\text{State-1}: W_{T_1} = \frac{R_{on}}{T_1} \left(\Delta q_{T_1,V_{in}} \right)^2 \\ &\text{State-2}: W_{T_2} = 0. \end{aligned} \tag{2.12}$$

The consumed energy during one operating cycle is obtained as:

$$W_T = \sum_{i=1}^{2} W_{T_i} = \frac{2R_{on}}{T} \left(\Delta q_{T_{V_{out}}}\right)^2 \tag{2.13}$$

From Figure 2.1, the consumed energy by R_{SC} for one operating cycle can be derived as:

$$W_T = \left(\langle I_{out} \rangle\right)^2 \cdot R_{SC} \cdot T = \frac{\left(\Delta q_{V_{out}}\right)^2}{T} \cdot R_{SC}. \tag{2.14}$$

Comparing Eqs. 2.13 and 2.14, the R_{SC} of the trivial topology is given by:

$$R_{SC} = 2R_{on}. \tag{2.15}$$

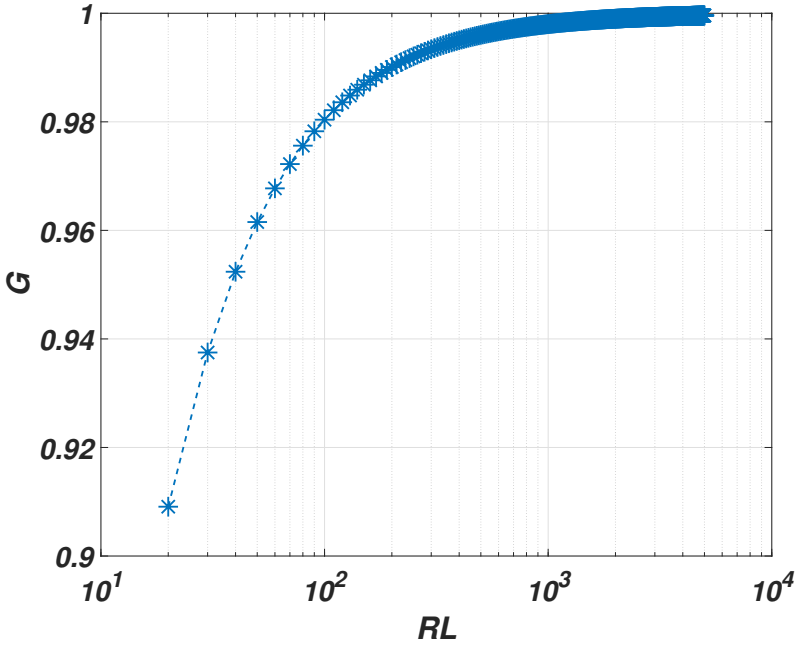
Finally, the relation of the average input/output voltage and current of the trivial topology can be expressed by a K-matrix:

$$\begin{bmatrix} \langle V_{in} \rangle \\ \langle I_{in} \rangle \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 2R_{on} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \langle V_{out} \rangle \\ -\langle I_{out} \rangle \end{bmatrix}. \tag{2.16}$$

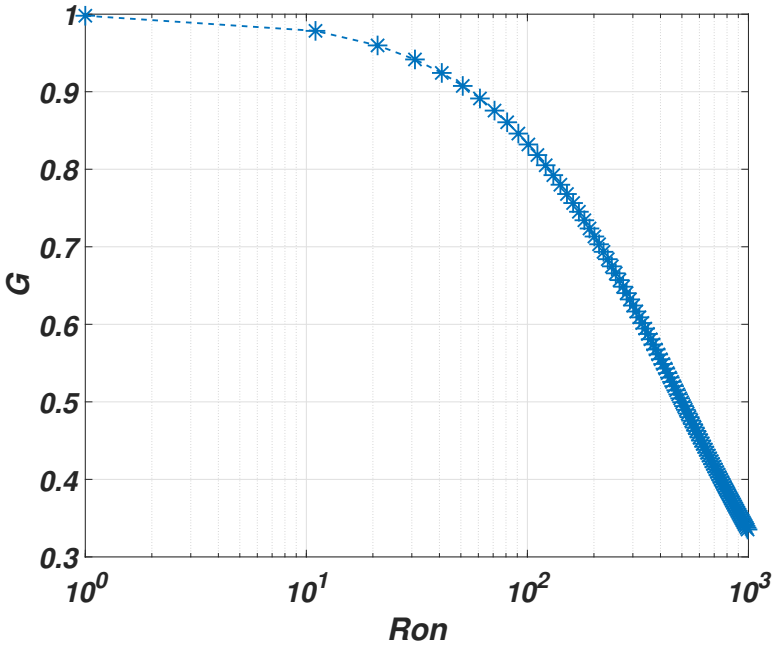
From the matrix, the output impedance R_{SC} and the output load R_L, the maximum efficiency and output voltage of the trivial topology, η_{max} and V_{out_max}, can be calculated by:

$$\eta_{max} = \frac{R_L}{R_L + R_{SC}} = \frac{R_L}{R_L + 2R_{on}}, \tag{2.17}$$

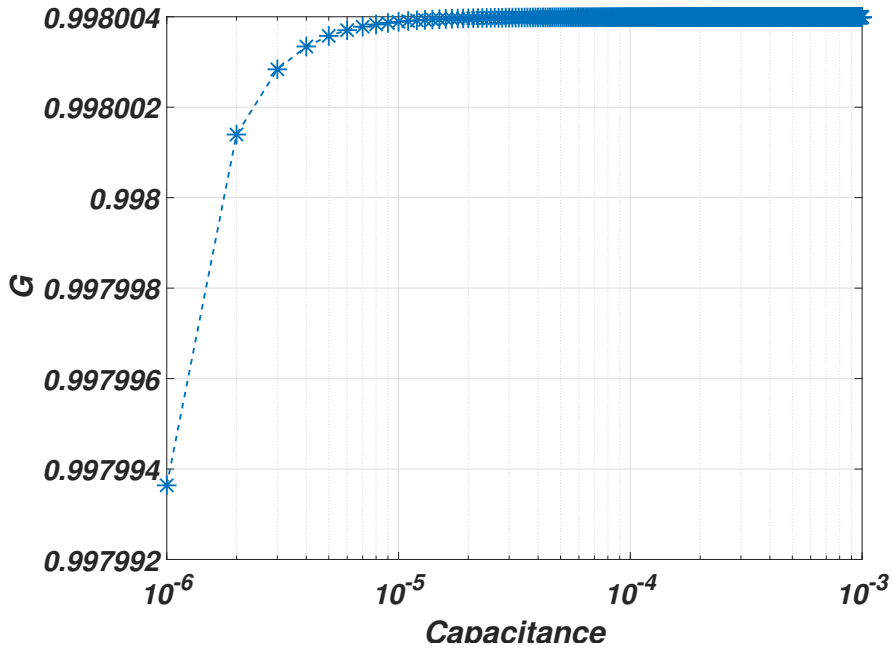
$$V_{out\_max} = \left(\frac{R_L}{R_L + 2R_{on}}\right) V_{in}. \tag{2.18}$$



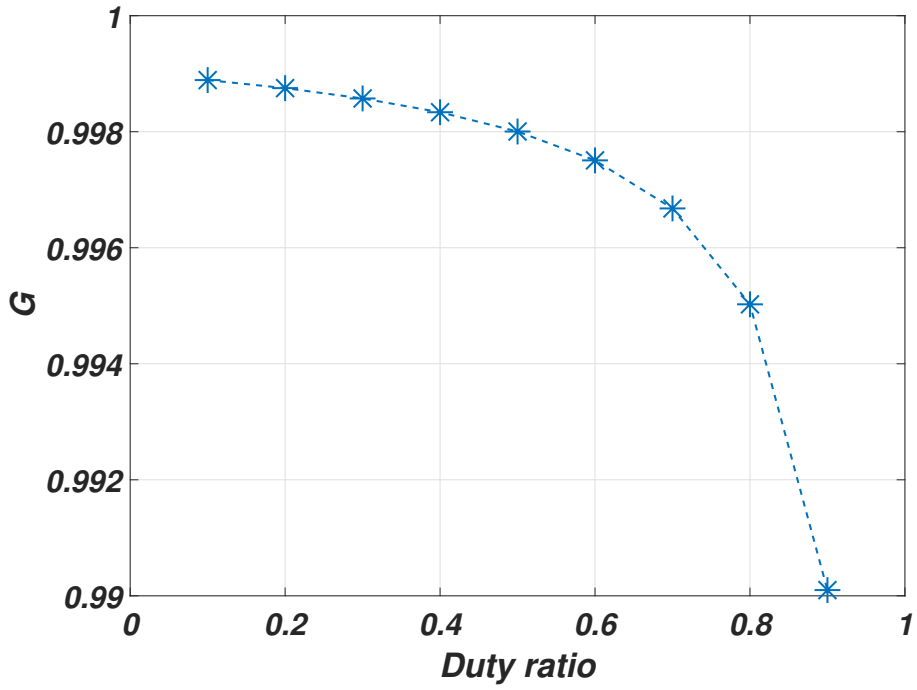
(a) Gain vs. load value (20Ω∼5kΩ)



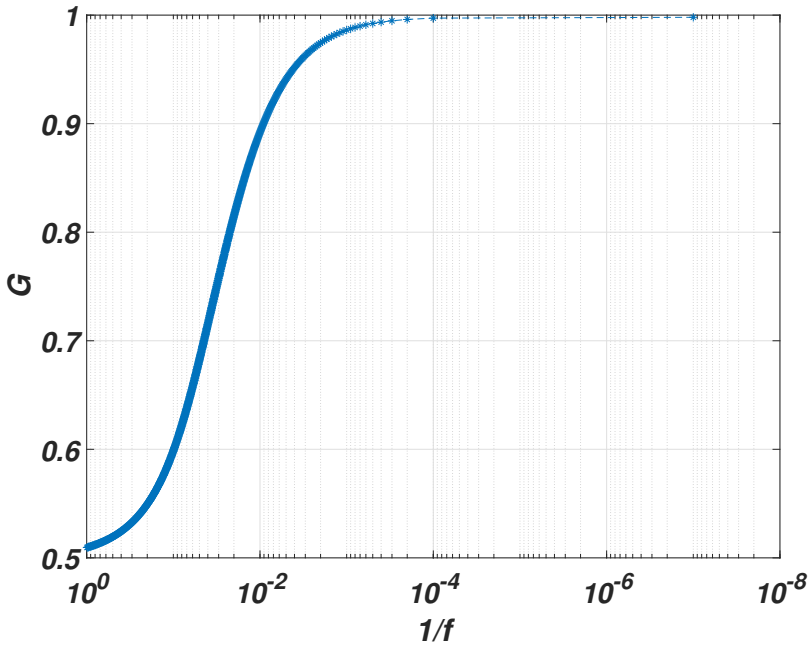
(b) Gain vs. on-resistor (10Ω∼1kΩ)



(c) Gain vs. capacitance (1μF$\sim$ 1000μF)



(d) Gain vs. duty ratio (0.1$\sim$0.9)



(e) Gain vs. frequency (1Hz∼10MHz)

Figure 2.4: Gain regulation with different parameters: (a) load value, (b) on-resistor, (c) capacitance, (d) duty ratio and (e) frequency.

Chapter 3

Comparing Topologies of Switched Capacitor DC-DC Converters

Until now, many different topologies of SC DC-DC converters have been suggested and developed [79, 80]. All of topologies have their own strengths and weaknesses. A selection standard is, therefore, necessary to provide an application with a efficient SC DC-DC converter.

In this chapter, topologies of SC DC-DC converters are sorted into a core topology group and a modified topology group. Two groups of topologies are analyzed based on the FE model. From the result of the modeling, the performances of the topologies are compared with their maximum output voltage and efficiency, output ripple voltage and circuit size at different conversion ratios from 2 to 20.

Additionally, this thesis mainly focuses on step-up types of the topologies.

3.1 Core Topology

A core topology of an SC DC-DC converter in this thesis is defiend as the topology that has the only one outermost mesh including its input and output ports. As this definition, Dickson, series-parallel and Fibonacci topology can be called core topologies.

Up to now, the core topologies have been utilized and researched in many commercial products because of being with their compact size and simple structure. Comparing the core topologies is able to make a standard to select them or an idea on upgrading and improving them.

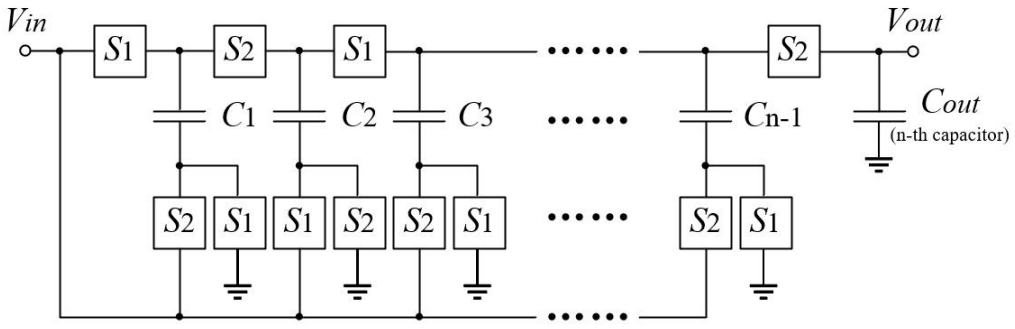


Figure 3.1: Dickson topology.

3.1.1 Dickson Topology (Dickson Charge Pump)

The Dickson topology (Dickson charge pump) was designed in 1976 by J. K. Dickson [9]. The proposed topology in [9] consisted of diodes and capacitors. Therefore, Figure3.1 shows the Dickson topology with n capacitors and $(3n-2)$ switches. The switches are changed into electrical switches ($S1$ and $S2$) such as MOSFET (metal-oxide-semiconductor field-effect transistor), where $n \geqq 2$. The switches, $S1$s and $S2$s, are oppositely turned on and off; when $S1$s are turned on, $S2$s are turned off, and vice versa. By this switching way, the Dickson topology with even-numbered n has the two instantaneous equivalent circuits as shown in Figure3.2. Until the topology reaches a steady state, the n-th capacitor has been fully charged to n times V_{in}, repeating State-1 and 2.

According to the principle of capacitor amp-second balance, the electric charge amount of the capacitor $C_k(k = 1, \cdots, n)$ of the Dickson topology can be expressed by:

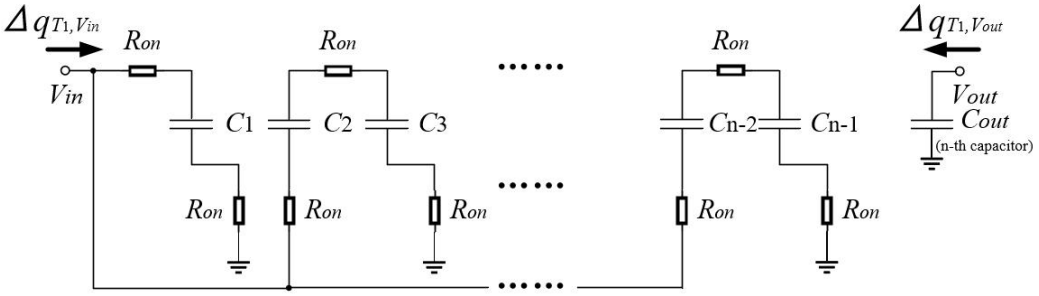
$$\sum_{i=1}^{2} \Delta q_{T_i}^{k} = 0, \tag{3.1}$$

where $\Delta q_{T_i}^{k}$ is the electric charge amount of k-th capacitor in State-i $(i = 1, 2)$.

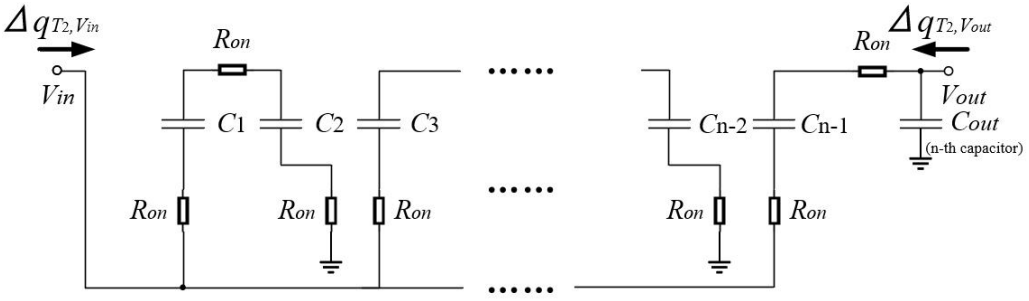
By setting the duty ratio D to 50%, T can be written as:

$$T = \sum_{i=1}^{2} T_i \quad \text{and} \quad T_1 = T_2 = \frac{T}{2}, \tag{3.2}$$

where $T_1 = (1-D)T$ and $T_2 = DT$.



(a) State-1



(b) State-2

Figure 3.2: Equivalent circuits of Dickson topology.

By using KCL, the relations of the electric charge amount of the input, output and capacitors at each operating state are calculated by:

$$\begin{aligned}
\text{State-1 :} &\Delta q_{T_1,V_{in}} = \Delta q^1_{T_1} - \Delta q^2_{T_1} - \Delta q^4_{T_1} - \cdots - \Delta q^{n-2}_{T_1}, \\
&\Delta q_{T_1,V_{out}} = \Delta q^n_{T_1} \\
\text{State-2 :} &\Delta q_{T_2,V_{in}} = \Delta q^2_{T_2} + \Delta q^4_{T_2} + \Delta q^6_{T_2} + \cdots - \Delta q^{n-1}_{T_2}, \\
&\Delta q_{T_2,V_{out}} = \Delta q^n_{T_2} + q^{n-1}_{T_2}
\end{aligned} \tag{3.3}$$

Using 3.3, the average input and output current is obtained as:

$$\langle I_{in} \rangle = -n \langle I_{out} \rangle , \tag{3.4}$$

where $\Delta q_{V_{out}} = -\Delta q^{n-1}_{T_1} = \Delta q^{n-1}_{T_2}$ and $\Delta q_{V_{in}} = -n\Delta q_{V_{out}}$.
From Eq. 3.4, the conversion ratio $m_{Dickson}$ is given by:

$$m_{Dickson} = n. \tag{3.5}$$

The consumed energy by on-resistors of switches during each operating state is calculated as:

$$\begin{aligned}
\text{State-1 }: W_{T_1} &= \frac{2R_{on}}{T_1}\left(\Delta q_{T_1}^{1}\right)^2 + \left(\frac{3n-6}{2}\right)\frac{2R_{on}}{T_1}\left(\Delta q_{T_1}^{n-1}\right)^2 \\
&= \left(2+\frac{3n-6}{2}\right)\frac{R_{on}}{T_1}\left(\Delta q_{V_{out}}\right)^2 \\
\text{State-2 }: W_{T_2} &= \left(\frac{3n-6}{2}\right)\frac{2R_{on}}{T_2}\left(\Delta q_{T_2}^{1}\right)^2 + \frac{2R_{on}}{T_2}\left(\Delta q_{T_2}^{n-1}\right)^2 \\
&= \left(2+\frac{3n-6}{2}\right)\frac{R_{on}}{T_2}\left(\Delta q_{V_{out}}\right)^2 .
\end{aligned} \tag{3.6}$$

The total consumed energy for one operating cycle is obtained as:

$$W_T = \sum_{i=1}^{2} W_{T_i} = \frac{(6n-4)R_{on}}{T}\left(\Delta q_{T_{V_{out}}}\right)^2 . \tag{3.7}$$

Comparing Eqs. 3.7 and 2.14, the R_{SC} of the Dickson topology is given by:

$$R_{SC} = (6n-4)R_{on}. \tag{3.8}$$

The K-matrix of the Dickson topology can be expressed by:

$$\begin{bmatrix} \langle V_{in}\rangle \\ \langle I_{in}\rangle \end{bmatrix} = \begin{bmatrix} \frac{1}{n} & 0 \\ 0 & n \end{bmatrix} \begin{bmatrix} 1 & (6n-4)R_{on} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \langle V_{out}\rangle \\ -\langle I_{out}\rangle \end{bmatrix}. \tag{3.9}$$

From above steps, the maximum efficiency and output voltage of the Dickson topology is calculated as:

$$\eta_{max} = \frac{R_L}{R_L + R_{SC}} = \frac{R_L}{R_L + (6n-4)R_{on}}, \tag{3.10}$$

$$V_{out\_max} = \left\{\frac{R_L}{R_L + (6n-4)R_{on}}\right\} V_{in}. \tag{3.11}$$

When the number of capacitors, n, is an odd number, R_{SC}, $m_{Dickson}$, η and V_{out_max} of the Dickson topology can be derived by substituing n into Eqs. 3.8, 3.10 and 3.11.

3.1.2 Series-Parallel Topology

Figure 3.3 shows the series-parallel topology consisting of $(n+1)$ capacitors and $(3n-1)$ switches, where $n \geqq 2$. The topology is operated by two states.

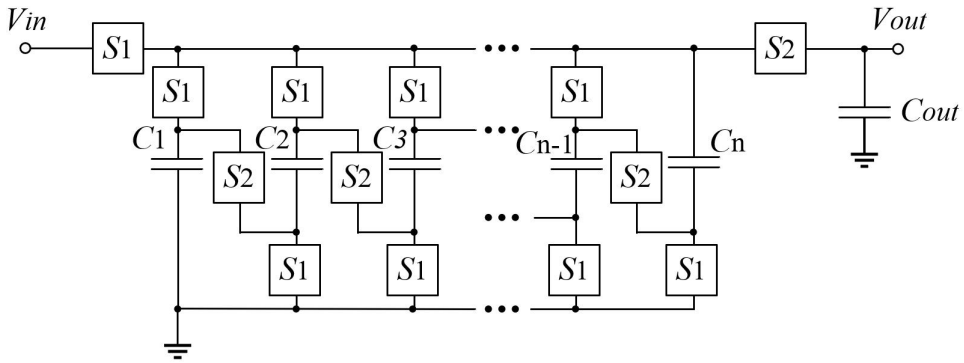
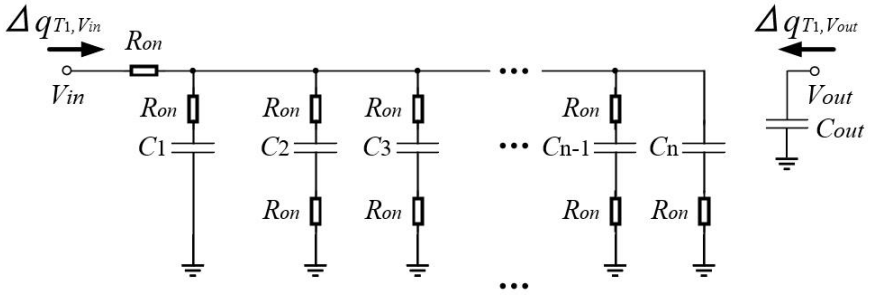
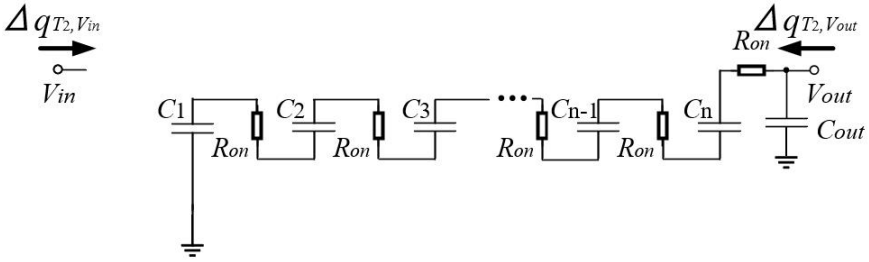


Figure 3.3: Series-Parallel topology.



(a) State-1



(b) State-2

Figure 3.4: Equivalent circuits of series-parallel topology.

When switches of $S1$ are turned on and switches of $S2$ are turned off in State-1, all capacitors except for the output capacitor C_{out} are charged to 1 times V_{in}, respectively. In State-2, $S1$s are turned off and $S2$s are turned on, by which all charged capacitors ($C_1 \sim C_n$) are connected in series and then the topology generates n times V_{in} as the output voltage. With this operation, the series-parallel topology has two instantaneous equivalent circuit as shown in Figure 3.4.

By using KCL, the relations of the electric charge amount of the input, output and capacitors at each operating state are calculated by:

$$\begin{aligned}
\text{State-1}: &\Delta q_{T_1,V_{in}} = \Delta q_{T_1}^1 + \cdots + \Delta q_{T_1}^m, \\
&\Delta q_{T_1,V_{out}} = \Delta q_{T1}^{out} \\
\text{State-2}: &\Delta q_{T_2,V_{in}} = 0, \\
&\Delta q_{T_2}^1 = \Delta q_{T_2}^2 = \Delta q_{T_2}^3 = \cdots = \Delta q_{T_2}^n, \\
&\Delta q_{T_2,V_{out}} = \Delta q_{T_2}^{out} + q_{T_2}^n
\end{aligned} \tag{3.12}$$

By setting the duty ratio D to 50%, T can be written as:

$$T = \sum_{i=1}^{2} T_i \quad \text{and} \quad T_1 = T_2 = \frac{T}{2}, \tag{3.13}$$

where $T_1 = (1-D)T$ and $T_2 = DT$.

According to the principle of capacitor amp-second balance, the relation of the average input and output current is given by:

$$\langle I_{in} \rangle = -n \langle I_{out} \rangle , \tag{3.14}$$

where $\Delta q_{V_{in}} = -n\Delta q_{V_{out}}$ and $\Delta q_{T_1}^1 = \Delta q_{T_1}^2 = \cdots = \Delta q_{T_1}^n$.

From Eq. 3.14, the conversion ratio $m_{S\text{-}P}$ is given by:

$$m_{S\text{-}P} = n. \tag{3.15}$$

The consumed energy by on-resistors of switches during each operating state is calculated as:

$$\begin{aligned}
\text{State-1}: W_{T_1} &= \frac{R_{on}}{T_1} \left(\Delta q_{T_1,V_{in}}\right)^2 + \frac{R_{on}}{T_1} \left(\Delta q_{T_1}^1\right)^2 + \frac{2(n-2)R_{on}}{T_1} \left(\Delta q_{T_1}^2\right)^2 \\
&\quad + \frac{R_{on}}{T_1} \left(\Delta q_{T_1}^n\right)^2 \\
&= \frac{(n^2+2n-2)R_{on}}{T_1} \left(\Delta q_{V_{out}}\right)^2 \\
\text{State-2}: W_{T_2} &= \frac{nR_{on}}{T_2} \left(\Delta q_{T_2}^n\right)^2 = \frac{nR_{on}}{T_2} \left(\Delta q_{V_{out}}\right)^2 .
\end{aligned} \tag{3.16}$$

With the 50% duty ratio, the total consumed energy during one operating cycle is obtained as:

$$W_T = \sum_{i=1}^{2} W_{T_i} = \frac{2(n^2+3n-2)R_{on}}{T} \left(\Delta q_{T_{V_{out}}}\right)^2 . \tag{3.17}$$

Comparing Eqs. 3.17 and 2.14, the R_{SC} of the series-parallel topology is given by:

$$R_{SC} = 2(n^2 + 3n - 2)R_{on}. \tag{3.18}$$

The K-matrix of the topology can be expressed by:

$$\begin{bmatrix} \langle V_{in} \rangle \\ \langle I_{in} \rangle \end{bmatrix} = \begin{bmatrix} \frac{1}{n} & 0 \\ 0 & n \end{bmatrix} \begin{bmatrix} 1 & 2(n^2 + 3n - 2)R_{on} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \langle V_{out} \rangle \\ -\langle I_{out} \rangle \end{bmatrix}. \tag{3.19}$$

From above steps, the maximum efficiency and output voltage of the series-parallel topology is calculated as:

$$\eta_{max} = \frac{R_L}{R_L + R_{SC}} = \frac{R_L}{R_L + 2(n^2 + 3n - 2)R_{on}}, \tag{3.20}$$

$$V_{out\_max} = \left\{ \frac{R_L}{R_L + 2(n^2 + 3n - 2)R_{on}} \right\} V_{in}. \tag{3.21}$$

In addition, the series-parallel topology can be operated as its step-down mode by changing the way that the capacitors are charged and discharged. Concretely, the capacitors in State-1 are connected in series and then charged to $\frac{1}{n}$ times V_{in}. In State-2, the charged capacitors are connected in parallel and transfer the energy to the output port or load with $\frac{1}{n}$ times V_{in} as the output voltage.

3.1.3 Fibonacci Topology

The Fibonacci topology as shown in Figure 3.5 consists of n cell of one capacitor and three switches. The Fibonacci topology has two operating modes: two operating states and three operating states modes. The switching rules of two operating modes are shown in Tab. 3.1 - 3.4. The two and three operating states modes are for the topology with the conversion ratio of Fibonacci number and non-Fibonacci number, respectively.

In two operating modes, the Fibonacci topology has two instantaneous equivalent circuits by the switching rule of Tab. 3.1 - 3.2. Figure 3.6 shows the topology with the conversion ratio of a Fibonacci number, where n is an odd number. Figure 3.7 depicts the topology with the conversion ratio of a non-Fibonacci number, where n is an even number.

Table 3.1: Switching rule: two operating states mode (n is an even number).

State	On	Off
1	Spm, Sgm (m=odd number), Ssk (k=even number)	Others
2	Spm, Sgm (m=even number), Ssk (k=odd number), So	Others

Table 3.2: Switching rule: two operating states mode (n is an odd number).

State	On	Off
1	Spm, Sgm (m=odd number), Ssk (k=even number), So	Others
2	Spm, Sgm (m=even number), Ssk (k=odd number)	Others

Table 3.3: Switching rule: three operating states mode (n is an even number).

State	On	Off
1	$Spm, Sgm(m = \text{odd number})$, $Ssk(k = \text{even number except } n)$	Ssn and Others
2	$Spm, Sgm(m = \text{even number})$, $Ssk(k = \text{odd number})$	Others
3	Ssk ($1 \leqq k \leqq n$), So	Others

Table 3.4: Switching rule: three operating states mode (n is an odd number).

State	On	Off
1	$Spm, Sgm(m = \text{odd number})$, $Ssk(k = \text{even number})$	Others
2	$Spm, Sgm(m = \text{even number})$, $Ssk(k = \text{odd number except } n)$	Ssn and Others
3	$Ssk(1 \leqq k \leqq n)$, So	Others

As a characteristic of this topology, it can generate various output voltages by the switching rules without adding any circuit components.

The following analysis is for the topology with the conversion ratio of 13 (Fibonacci number). By using KCL, the relations of the electric charge amount of the input, output and capacitors at each operating state are calculated by:

$$\begin{aligned}
\text{State-1 :}&\Delta q_{T_1,V_{in}} = \Delta q^1_{T1} - \Delta q^2_{T1},\\
&\Delta q^2_{T1} = -\Delta q^3_{T1},\\
&\Delta q^2_{T1} = -\Delta q^3_{T1} + \Delta q^4_{T1},\\
&\Delta q^4_{T1} = -\Delta q^5_{T1},\\
&\Delta q_{T_1,V_{out}} = \Delta q^6_{T1}\\
\text{State-2 :}&\Delta q_{T_2,V_{in}} = -\Delta q^1_{T_2},\\
&\Delta q^1_{T_2} = -\Delta q^2_{T_2} + \Delta q^3_{T_2},\\
&\Delta q^3_{T_2} = -\Delta q^4_{T_2} + \Delta q^5_{T_2},\\
&\Delta q^5_{T_2} = -\Delta q^6_{T_2},\\
&\Delta q_{T_2,V_{out}} = \Delta q^6_{T_2} + \Delta q^5_{T_2}
\end{aligned} \tag{3.22}$$

By setting the duty ratio D to 50%, T can be written as:

$$T = \sum_{i=1}^{2} T_i \quad \text{and} \quad T_1 = T_2 = \frac{T}{2}, \tag{3.23}$$

where $T_1 = (1-D)T$ and $T_2 = DT$.

According to the principle of capacitor amp-second balance, the relation of the average input and output current is given by:

$$\langle I_{in} \rangle = -13 \langle I_{out} \rangle , \tag{3.24}$$

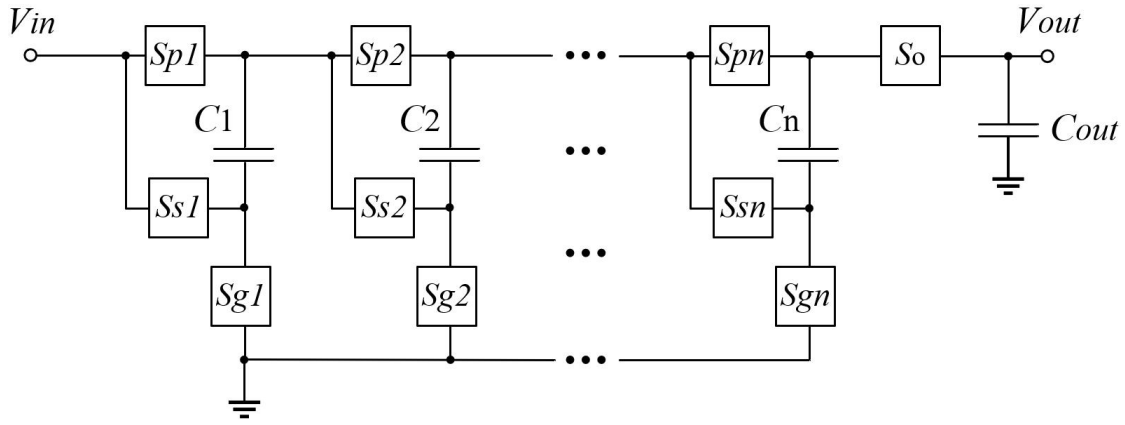
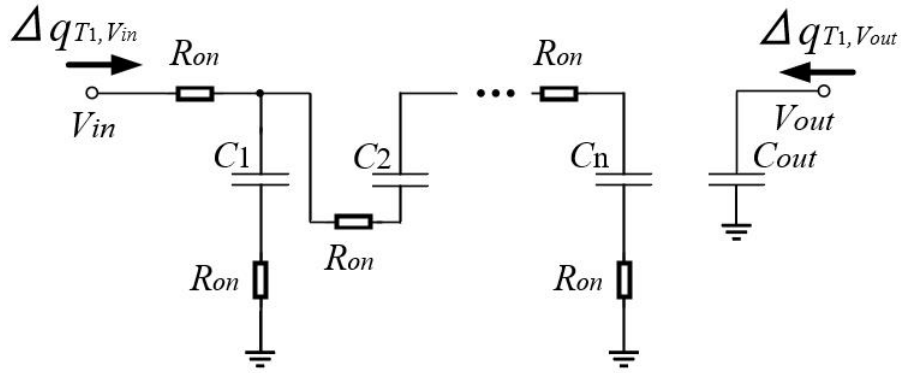
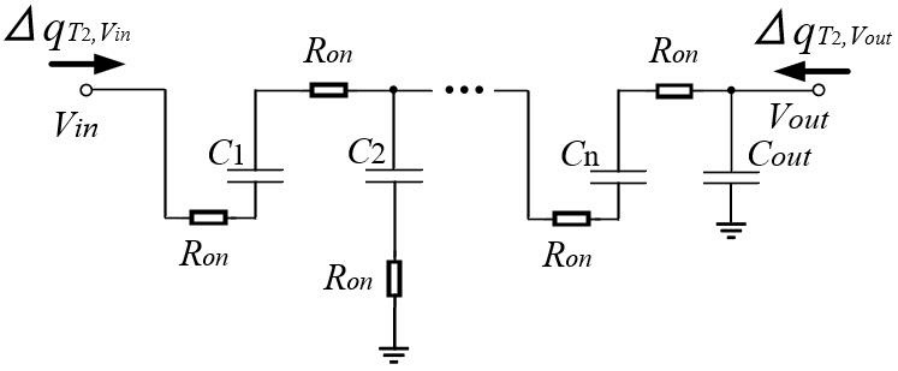


Figure 3.5: Fibonacci topology.



(a) State-1



(b) State-2

Figure 3.6: Equivalent circuits of Fibonacci topology (Fibonacci number).

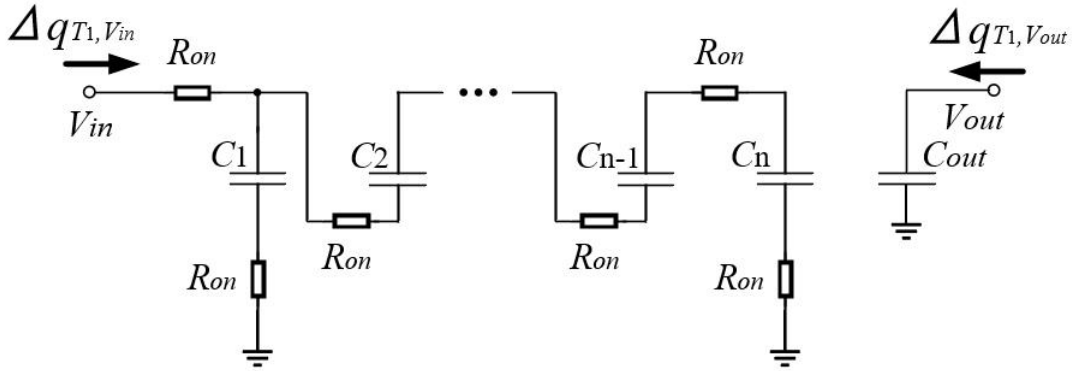
where $\Delta q_{V_{in}} = -13\Delta q_{V_{out}}$ and $\Delta q_{V_{out}} = -\Delta q_{T_1}^5 = \Delta q_{T_2}^5$.

From Eq. 3.24, the conversion ratio m_{fibo} is given by:

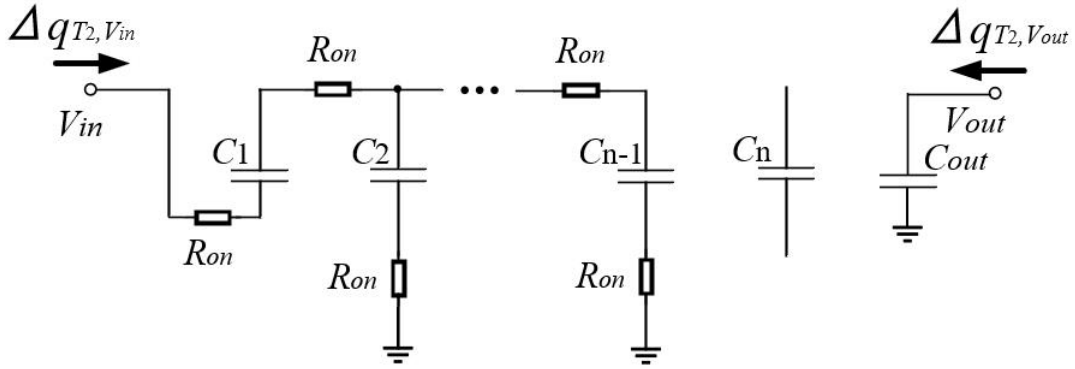
$$m_{fibo} = 13. \tag{3.25}$$

The consumed energy by on-resistors of switches during each operating state is calculated as:

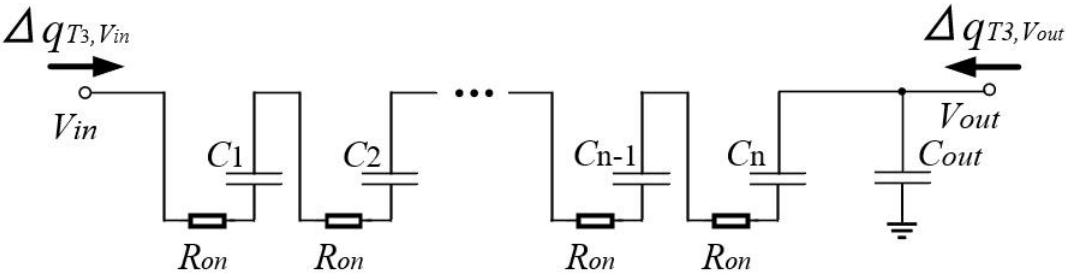
$$\begin{aligned} \text{State-1 :} W_{T_1} &= \frac{R_{on}}{T_1}\left\{\left(\Delta q_{T_1}^1 - \Delta q_{T_1}^2\right)^2 + \left(\Delta q_{T_1}^1\right)^2 + 2\left(\Delta q_{T_1}^2\right)^2 + \left(\Delta q_{T_1}^3\right)^2 \right. \\ &\quad \left. +3\left(\Delta q_{T_1}^4\right)^2\right\} \\ &= \frac{114R_{on}}{T_1}\left(\Delta q_{V_{out}}\right)^2 \end{aligned}$$



(a) State-1



(b) State-2



(c) State-3

Figure 3.7: Equivalent circuits of Fibonacci topology (non-Fibonacci number).

$$\begin{aligned}\text{State-2 }: W_{T_2} &= \frac{R_{on}}{T_1}\left\{2\left(\Delta q_{T2}^{1}\right)^2+\left(\Delta q_{T2}^{2}\right)^2+2\left(\Delta q_{T2}^{3}\right)^2+\left(\Delta q_{T2}^{4}\right)^2\right. \\ &\quad \left.+2\left(\Delta q_{T2}^{5}\right)^2\right\} \\ &= \frac{70R_{on}}{T_2}\left(\Delta q_{V_{out}}\right)^2.\end{aligned} \tag{3.26}$$

With the 50% duty ratio, the total consumed energy during one operating cycle is obtained as:

$$W_T = \sum_{i=1}^{2} W_{T_i} = \frac{368R_{on}}{T}\left(\Delta q_{T_{V_{out}}}\right)^2. \tag{3.27}$$

Comparing Eqs. 3.27 and 2.14, the R_{SC} of the Fibonacci topology ($m_{fibo} = 13$) is given by:

$$R_{SC} = 368R_{on}. \tag{3.28}$$

The K-matrix of the topology ($m_{fibo} = 13$) can be expressed by:

$$\begin{bmatrix}\langle V_{in}\rangle \\ \langle I_{in}\rangle\end{bmatrix} = \begin{bmatrix}\frac{1}{13} & 0 \\ 0 & 13\end{bmatrix}\begin{bmatrix}1 & 368R_{on} \\ 0 & 1\end{bmatrix}\begin{bmatrix}\langle V_{out}\rangle \\ -\langle I_{out}\rangle\end{bmatrix}. \tag{3.29}$$

From above steps, the maximum efficiency and output voltage of the Fibonacci topology ($m_{fibo} = 13$) is calculated as:

$$\eta_{max} = \frac{R_L}{R_L + R_{SC}} = \frac{R_L}{R_L + 368R_{on}}, \tag{3.30}$$

$$V_{out\_max} = \left\{\frac{R_L}{R_L + 368R_{on}}\right\} V_{in}. \tag{3.31}$$

Next, the following analysis is for the topology with the conversion ratio of 20 (non-Fibonacci number).

$$\begin{aligned}
\text{State-1 :}&\Delta q_{T_1,V_{in}} = \Delta q^1_{T_1} - \Delta q^2_{T_1},\\
&\Delta q^2_{T_1} = -\Delta q^3_{T_1},\\
&\Delta q^2_{T_1} = -\Delta q^3_{T_1} + \Delta q^4_{T_1},\\
&\Delta q^4_{T_1} = -\Delta q^5_{T_1},\\
&\Delta q_{T_1,V_{out}} = \Delta q^6_{T_1}\\
\text{State-2 :}&\Delta q_{T_2,V_{in}} = -\Delta q^1_{T_2},\\
&\Delta q^1_{T_2} = -\Delta q^2_{T_2} + \Delta q^3_{T_2},\\
&\Delta q^3_{T_2} = -\Delta q^4_{T_2} + \Delta q^5_{T_2},\\
&\Delta q^5_{T_2} = 0,\\
&\Delta q_{T_2,V_{out}} = \Delta q^6_{T_2}\\
\text{State-3 :}&\Delta q_{T_3,V_{in}} = -\Delta q^1_{T_3},\\
&\Delta q^1_{T_3} = \Delta q^2_{T3} = \Delta q^3_{T_3} = \Delta q^4_{T_3} = \Delta q^5_{T_3}\\
&\Delta q_{T_3,V_{out}} = \Delta q^6_{T_3} + \Delta q^5_{T_3}
\end{aligned} \tag{3.32}$$

By setting the duty ratio D to $\frac{1}{3}$, T can be written as:

$$T = \sum_{i=1}^{3} T_i \quad \text{and} \quad T_1 = T_2 = T_3 = \frac{T}{3}, \tag{3.33}$$

where $T_1 = D_1 T$ for state-1, $T_2 = D_2 T$ for state-2 and $T_3 = D_3 T$ for state-3.

According to the principle of capacitor amp-second balance, the relation of the average input and output current is given by:

$$\langle I_{in} \rangle = -20 \langle I_{out} \rangle , \tag{3.34}$$

where $\Delta q_{V_{in}} = -20 \Delta q_{V_{out}}$ and $\Delta q_{V_{out}} = -\frac{1}{8}\Delta q^1_{T_1} = -\frac{1}{4}\Delta q^2_{T_1} = \frac{1}{7}\Delta q^1_{T_2} = \Delta q^5_{T_3}$.
From Eq. 3.34, the conversion ratio m_{fibo} is given by:

$$m_{fibo} = 20. \tag{3.35}$$

The consumed energy by on-resistors of switches during each operating state is calculated as:

$$\begin{aligned}
\text{State-1 }: W_{T_1} &= \frac{R_{on}}{T_1}\left\{\left(\Delta q_{T_1}^1 - \Delta q_{T_1}^2\right)^2 + \left(\Delta q_{T_1}^1\right)^2 + 2\left(\Delta q_{T_1}^2\right)^2 + \left(\Delta q_{T_1}^3\right)^2 \right. \\
&\quad \left. +3\left(\Delta q_{T_1}^4\right)^2\right\} \\
&= \frac{252R_{on}}{T_1}\left(\Delta q_{V_{out}}\right)^2 \\
\text{State-2 }: W_{T_2} &= \frac{R_{on}}{T_1}\left\{2\left(\Delta q_{T_2}^1\right)^2 + \left(\Delta q_{T_2}^2\right)^2 + 3\left(\Delta q_{T_2}^3\right)^2\right\} \\
&= \frac{135R_{on}}{T_2}\left(\Delta q_{V_{out}}\right)^2 \\
\text{State-2 }: W_{T_3} &= \frac{6R_{on}}{T_3}\Delta q_{V_{out}}
\end{aligned} \tag{3.36}$$

With the $\frac{1}{3}$ duty ratio, the total consumed energy during one operating cycle is obtained as:

$$W_T = \sum_{i=1}^{3} W_{T_i} = \frac{1179R_{on}}{T}\left(\Delta q_{T_{V_{out}}}\right)^2. \tag{3.37}$$

Comparing Eqs. 3.37 and 2.14, the R_{SC} of the Fibonacci topology ($m_{Fibo} = 20$) is given by:

$$R_{SC} = 1179R_{on}. \tag{3.38}$$

The K-matrix of the topology ($m_{Fibo} = 20$) can be expressed by:

$$\begin{bmatrix}\langle V_{in}\rangle \\ \langle I_{in}\rangle\end{bmatrix} = \begin{bmatrix}\frac{1}{20} & 0 \\ 0 & 20\end{bmatrix}\begin{bmatrix}1 & 1179R_{on} \\ 0 & 1\end{bmatrix}\begin{bmatrix}\langle V_{out}\rangle \\ -\langle I_{out}\rangle\end{bmatrix}. \tag{3.39}$$

From above steps, the maximum efficiency and output voltage of the Fibonacci topology ($m_{Fibo} = 20$) is calculated as:

$$\eta_{max} = \frac{R_L}{R_L + R_{SC}} = \frac{R_L}{R_L + 1179R_{on}}, \tag{3.40}$$

$$V_{out\_max} = \left(\frac{R_L}{R_L + 1179R_{on}}\right)V_{in}. \tag{3.41}$$

Using the same analysis way as the above two cases, the R_{SC} of the Fibonacci topology with the conversion ratio from 2 to 20 can be calculated as shown in Tab. 3.5.

Table 3.5: Conversion ratio and R_{SC} of Fibonacci topology.

m_{Fibo}	R_{SC}
2	$8R_{on}$
3	$20R_{on}$
4	$42R_{on}$
5	$54R_{on}$
6	$96R_{on}$
7	$132R_{on}$
8	$140R_{on}$
9	$228R_{on}$
10	$282R_{on}$
11	$339R_{on}$
12	$403R_{on}$
13	$368R_{on}$
14	$573R_{on}$
15	$678R_{on}$
16	$852R_{on}$
17	$858R_{on}$
18	$1062R_{on}$
19	$1065R_{on}$
20	$1179R_{on}$

3.2 Modified Topology

There are various ways to modify SC DC-DC converters to improve their performance: changing or inserting circuit components, different operation ways, merging two or more SC DC-DC converters, etc. This chapter focuses on the modifying way of combining two converters. Typically, there are three ways to link topologies of SC DC-DC converters. In the three modification ways, the topologies are connected in cascaded, symmetrical and cross-connected construction, respectively. The following three subchapters deal with three modified topologies.

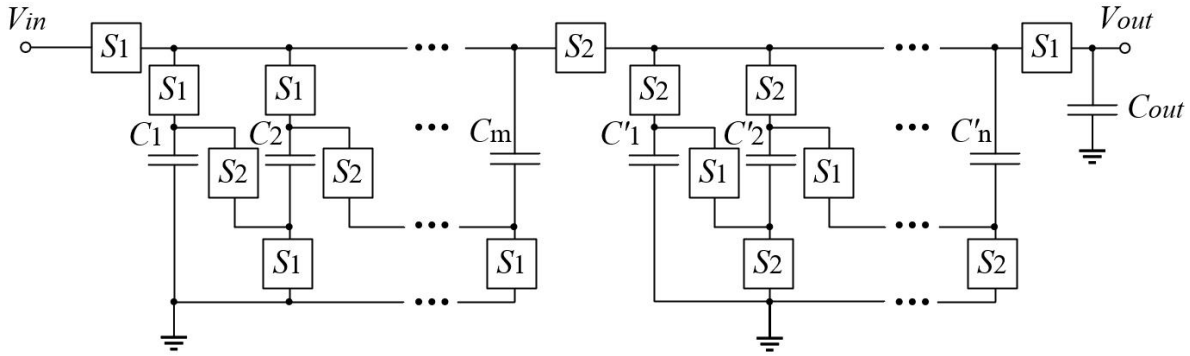


Figure 3.8: SCVM topology.

3.2.1 Switched Capacitor Voltage Multiplier (SCVM) Topology

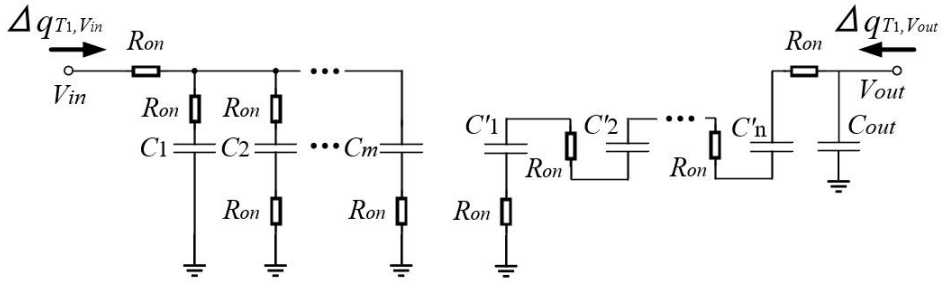
The topology modified by the cascaded construction is to link two or more topologies in series. The representative example is the switched capacitor voltage multiplier (SCVM) topology [14, 81]. The SCVM topology can consist of two or more than two series-parallel topologies connected in series.

Figure 3.8 shows the SCVM topology consisting of two series-parallel topologies with the conversion ratio of $m \times n$, where m and n are the number of capacitors in the first and second cell, respectively. The switches S_1 and S_2 with the on-resistor R_{on} are oppositely turned on and off, by which the SCVM topology has two instantaneous equivalent circuits as shown in Figure 3.9.

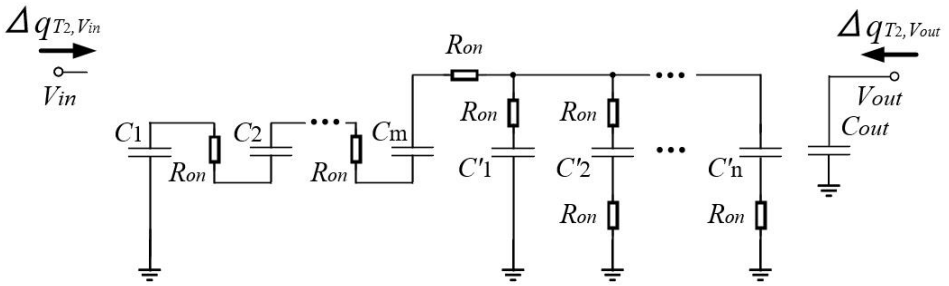
By using KCL, the relations of the electric charge amount of the input, output and capacitors at each operating state are calculated by:

$$\begin{aligned}
\text{State-1 :} & \Delta q_{T_1,V_{in}} = \Delta q^1_{T_1} + \Delta q^2_{T_1} + \Delta q^3_{T_1} + \cdots + \Delta q^m_{T_1}, \\
& \Delta k^1_{T_1} = \cdots = \Delta k^n_{T_1} \\
& \Delta q_{T_1,V_{out}} = \Delta k^n_{T_1} + \Delta q^{out}_{T_1} \\
\text{State-2 :} & \Delta q_{T_2,V_{in}} = 0, \\
& \Delta q^m_{T_2} = \Delta k^1_{T_2} + \Delta k^2_{T_2} + \Delta k^3_{T_2} + \cdots + \Delta k^n_{T_2} \\
& \Delta q^1_{T_2} = \cdots = \Delta q^m_{T_2}, \quad \Delta q_{T_2,V_{out}} = \Delta q^{out}_{T2},
\end{aligned} \tag{3.42}$$

where $\Delta k^k_{T_i}$ means the electric charges amount of k-th capacitor (C'k) in the second cell (n cell) during State-i(i=1,2).



(a) State-1



(b) State-2

Figure 3.9: Equivalent circuits of SCVM topology.

By setting the duty ratio D to 50%, T can be written as:

$$T = \sum_{i=1}^{2} T_i \quad \text{and} \quad T_1 = T_2 = \frac{T}{2}, \tag{3.43}$$

where $T_1 = (1 - D)T$ and $T_2 = DT$.

According to the principle of capacitor amp-second balance, the relation of the average input and output current is given by:

$$\langle I_{in} \rangle = -mn \langle I_{out} \rangle , \tag{3.44}$$

where $\Delta q_{V_{in}} = -mn\Delta q_{V_{out}}$, $\Delta q_{V_{out}} = \Delta k^n_{T_1}$, $\Delta q_{V_{in}} = -m\Delta q^m_{T_2}$ and $\Delta q^m_{T_2} = n\Delta k^n_{T_1}$. From Eq. 3.44, the conversion ratio $m_{S\text{-}P}$ is given by:

$$m_{SCVM} = mn. \tag{3.45}$$

The consumed energy by on-resistors of switches during each operating state is calculated as:

$$\begin{aligned}
\text{State-1 }: W_{T_1} &= \frac{R_{on}}{T_1}\left(\Delta q_{T_1,V_{in}}\right)^2 + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^1\right)^2 + \frac{2(m-2)R_{on}}{T_1}\left(\Delta q_{T_1}^2\right)^2 \\
&\quad + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^m\right)^2 \\
&= \frac{\left(m^2n^2 + 2mn^2 - 2n^2 + 2n\right)R_{on}}{T_1}\left(\Delta q_{V_{out}}\right)^2 \\
\text{State-2 }: W_{T_2} &= \frac{mR_{on}}{T_2}\left(\Delta q_{T_2}^1\right)^2 + \frac{R_{on}}{T_2}\left(\Delta k_{T_2}^1\right)^2 + \frac{2(n-2)R_{on}}{T_1}\left(\Delta k_{T_2}^2\right)^2 \\
&\quad + \frac{R_{on}}{T_1}\left(\Delta k_{T_1}^n\right)^2 \\
&= \frac{\left(mn^2 + 2n - 4\right)R_{on}}{T_1}\left(\Delta q_{V_{out}}\right)^2
\end{aligned} \tag{3.46}$$

With the 50% duty ratio, the total consumed energy during one operating cycle is obtained as:

$$W_T = \sum_{i=1}^{2} W_{T_i} = \frac{\left(2m^2n^2 + 6mn^2 - 4n^2 + 6n - 8\right)R_{on}}{T}\left(\Delta q_{T_{V_{out}}}\right)^2. \tag{3.47}$$

Comparing Eqs. 3.47 and 2.14, the R_{SC} of the SCVM topology is given by:

$$R_{SC} = \left(2m^2n^2 + 6mn^2 - 4n^2 + 6n - 8\right)R_{on}. \tag{3.48}$$

From Eq. 3.48, it is verified that the less the SCVM topology has capacitors in n cell, the smaller R_{RC} it has.

The K-matrix of the topology can be expressed by:

$$\begin{bmatrix}\langle V_{in}\rangle \\ \langle I_{in}\rangle\end{bmatrix} = \begin{bmatrix}\frac{1}{mn} & 0 \\ 0 & mn\end{bmatrix}\begin{bmatrix}1 & \left(2m^2n^2 + 6mn^2 - 4n^2 + 6n - 8\right)R_{on} \\ 0 & 1\end{bmatrix}\begin{bmatrix}\langle V_{out}\rangle \\ -\langle I_{out}\rangle\end{bmatrix}. \tag{3.49}$$

From above steps, the maximum efficiency and output voltage of the SCVM topology is calculated as:

$$\eta_{max} = \frac{R_L}{R_L + R_{SC}} = \frac{R_L}{R_L + \left(2m^2n^2 + 6mn^2 - 4n^2 + 6n - 8\right)R_{on}}. \tag{3.50}$$

$$V_{out\_max} = \left\{\frac{R_L}{R_L + \left(2m^2n^2 + 6mn^2 - 4n^2 + 6n - 8\right)R_{on}}\right\}V_{in}. \tag{3.51}$$

3.2.2 Symmetrical Dickson Topology

To improve the response speed and the power efficiency of SC DC-DC converters, it is a solution to combine two topologies of those in a symmetrical structure. An SC DC-DC converter with symmetrical structure can charge its output capacitor and transfer the converted power to its output load during all operating states. Also, this operation lead to decrease in the output capacitor capacitance of the converter [82, 83].

Figure 3.10 shows the symmetrical Dickson topology. The topology consists of two normal Dickson topology cells with one output capacitor. Each cell has $(n-1)$ capacitors and $(3n-1)$ switches with the on-resistor R_{on}, where $n \geqq 2$. The topology is operated by two states. The cell 1 and 2 are oppositely operated, which means that in the state-1, the cell 1 transfers the stepped-up voltage to the output while the cell 2 charges the flying capacitors and vice versa in the state-2. With this operation, the symmetrical Dickson topology has two symmetric instantaneous equivalent circuits as shown Figure 3.11. The switches $S1$ and $S2$ are turned on and off in state-1, respectively, and vice versa in state-2.

By using KCL, the relations of the electric charge amount of the input, output and capacitors at each operating state are calculated by:

$$\begin{aligned}
\text{State-1 :}\Delta q_{T_1,V_{in}} &= \Delta q^1_{T_1} - \Delta q^2_{T_1} - \Delta q^4_{T_1} - \cdots - \Delta q^{n-2}_{T_1} \\
&\quad + \Delta k^2_{T_1} + \Delta k^4_{T_1} + \Delta k^6_{T_1} + \cdots + \Delta k^{n-2}_{T_1} - \Delta k^{n-2}_{T_1} \\
\Delta q_{T_1,V_{out}} &= \Delta k^{n-1}_{T_1} + \Delta q^{out}_{T_1} \\
\text{State-2 :}\Delta q_{T_2,V_{in}} &= \Delta k^1_{T_2} - \Delta k^2_{T_2} - \Delta k^4_{T_2} - \cdots - \Delta k^{n-2}_{T_2} \\
&\quad + \Delta q^2_{T_2} + \Delta q^4_{T_2} + \Delta q^6_{T_2} + \cdots + \Delta q^{n-2}_{T_2} - \Delta q^{n-2}_{T_2} \\
\Delta q_{T_2,V_{out}} &= \Delta q^{n-1}_{T_1} + \Delta q^{out}_{T_2}
\end{aligned} \tag{3.52}$$

where $\Delta k^k_{T_i}$ means the electric charges amount of k-th capacitor (C'k) in the cell 2 (n cell) during State-i(i=1,2).

By setting the duty ratio D to 50%, T can be written as:

$$T = \sum_{i=1}^{2} T_i \quad \text{and} \quad T_1 = T_2 = \frac{T}{2}, \tag{3.53}$$

where $T_1 = (1-D)T$ and $T_2 = DT$.

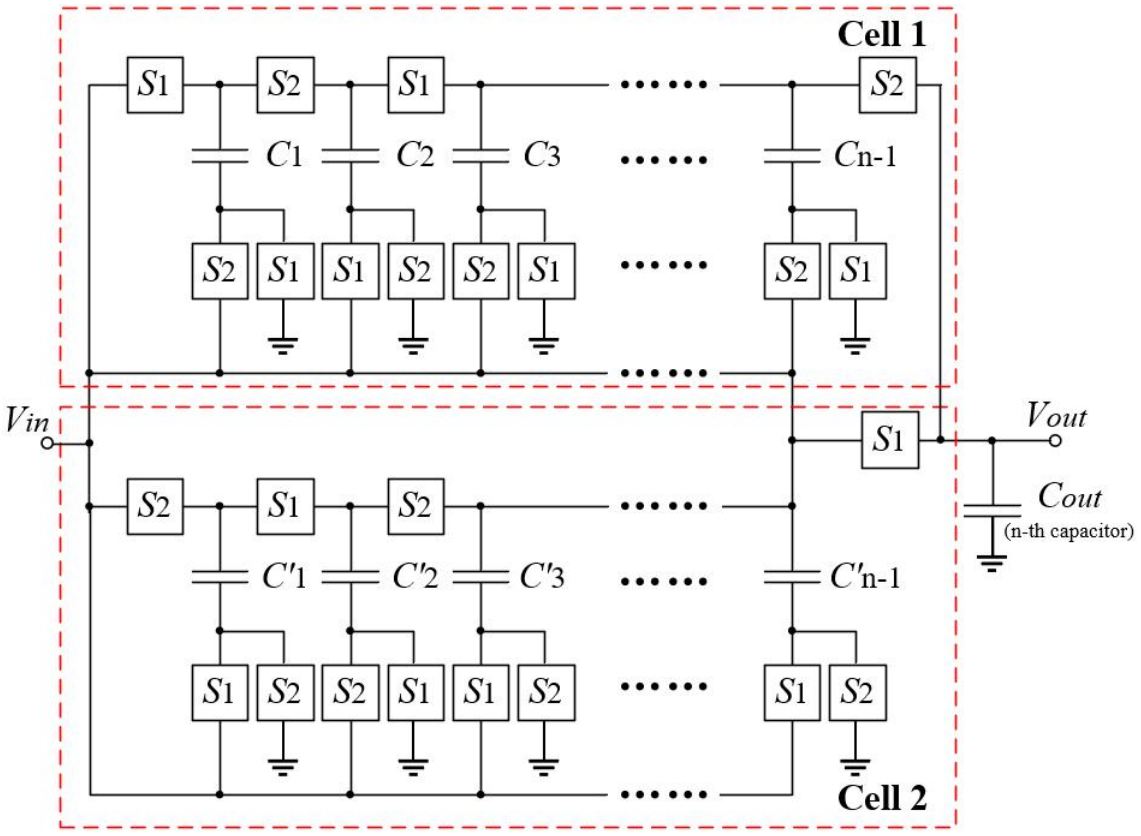
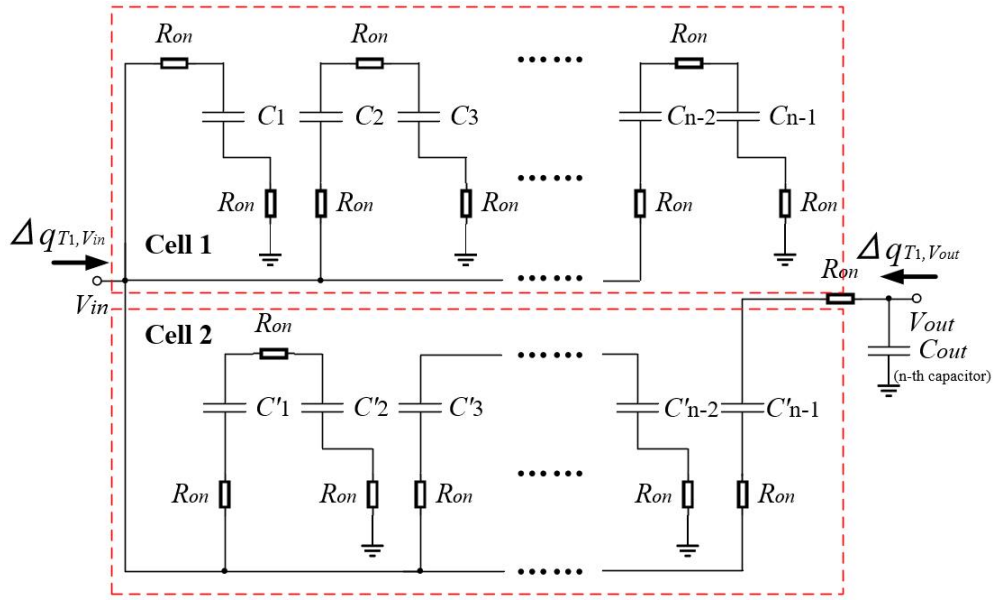
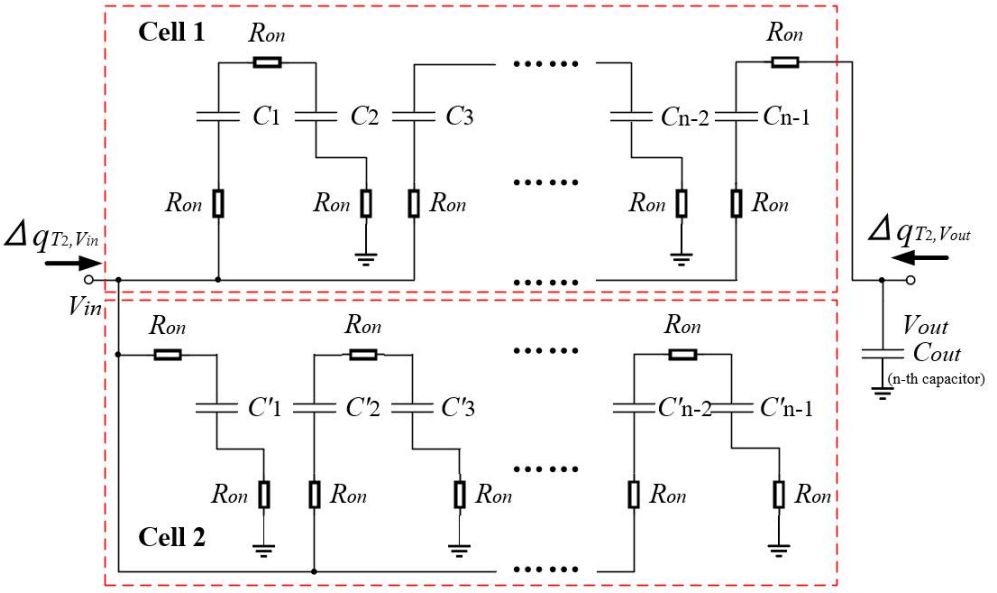


Figure 3.10: Symmetrical Dickson topology.



(a) State-1



(b) State-2

Figure 3.11: Instantaneous equivalent circuits of symmetrical Dickson topology.

According to the principle of capacitor amp-second balance, the relation of the average input and output current is given by:

$$\langle I_{in} \rangle = -n \langle I_{out} \rangle , \tag{3.54}$$

where $\Delta q_{V_{in}} = -n\Delta q_{V_{out}}$, $\Delta q_{T_1}^k = \Delta k_{T_2}^k (1 \leqq k \leqq n-1)$ and $\Delta q_{V_{out}} = 2\Delta k_{T_1}^{n-1}$. From Eq. 3.54, the conversion ratio $m_{symDickson}$ is given by:

$$m_{symDickson} = n. \tag{3.55}$$

The consumed energy by on-resistors of switches during each operating state is calculated as:

$$\begin{aligned} \text{State-1 :} W_{T_1} &= \frac{2R_{on}}{T_1} \left(\Delta q_{T_1}^1\right)^2 + \frac{3R_{on}}{T_1} \left(\Delta q_{T_1}^2\right)^2 + \frac{3R_{on}}{T_1} \left(\Delta q_{T_1}^4\right)^2 + \cdots \\ &\quad + \frac{3R_{on}}{T_1} \left(\Delta q_{T_1}^{n-2}\right)^2 + \frac{3R_{on}}{T_1} \left(\Delta k_{T_1}^2\right)^2 + \frac{3R_{on}}{T_1} \left(\Delta k_{T_1}^4\right)^2 + \cdots \\ &\quad + \frac{2R_{on}}{T_1} \left(\Delta k_{T_1}^{n-1}\right)^2 \\ &= \left(1 + \frac{3n-6}{4}\right) \frac{R_{on}}{T_1} \left(\Delta q_{V_{out}}\right)^2 \end{aligned} \tag{3.56}$$

$$\text{State-2 :} W_{T_2} = W_{T_1}$$

With the 50% duty ratio, the total consumed energy during one operating cycle is obtained as:

$$\begin{aligned} W_T &= \sum_{i=1}^{2} W_{T_i} = 2W_{T_1} = \left(2 + \frac{3n-6}{2}\right) \frac{R_{on}}{T_1} \left(\Delta q_{T_{V_{out}}}\right)^2 \\ &= \frac{(3n-2)R_{on}}{T} \left(\Delta q_{T_{V_{out}}}\right)^2 . \end{aligned} \tag{3.57}$$

Comparing Eqs. 3.57 and 2.14, R_{SC} of the symmetrical Dickson topology is given by:

$$R_{SC} = (3n-2)\, R_{on}. \tag{3.58}$$

The K-matrix of the topology can be expressed by:

$$\begin{bmatrix} \langle V_{in} \rangle \\ \langle I_{in} \rangle \end{bmatrix} = \begin{bmatrix} \frac{1}{n} & 0 \\ 0 & n \end{bmatrix} \begin{bmatrix} 1 & (3n-2)\, R_{on} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \langle V_{out} \rangle \\ -\langle I_{out} \rangle \end{bmatrix} . \tag{3.59}$$

From above steps, the maximum efficiency and output voltage of the symmetrical Dickson topology is calculated as:

$$\eta_{max} = \frac{R_L}{R_L + R_{SC}} = \frac{R_L}{R_L + (3n-2)\, R_{on}}. \tag{3.60}$$

$$V_{out\_max} = \left\{ \frac{R_L}{R_L + (3n-2)\,R_{on}} \right\} V_{in}. \tag{3.61}$$

3.2.3 Cross-connected Fibonacci Topology

The cross-connected Fibonacci topology as shown in Figure 3.12. The topology consists of two Fibonacci topologies and has the cross connection. More precisely, the switches Ssn and Ysn are cross-connected to the capacitors C'_{n-1} and C_{n-1}, respectively. This topology is composed of $2n$ capacitors, one output capacitor and $(6n+2)$ switches, where $(n \geqq 2)$.

The structure feature of the cross-connection leads to the lower output ripple voltage and the decrease of circuit components, comparing with the normal Fibonacci topology at the same conversion ratio. This comparison is discussed in section 3.3.2. The cross-connected topology is operated by two operation modes based on the switching rule in Table 3.6 and 3.7. With the switching rule, the cross-connected topology has two instantaneous equivalent circuits as depicted in Figure 3.13. The distinguished feature of the cross-connected topology is that it can generate 2 times higher output voltage than the normal Fibonacci one with the same stage number, where a stage consists of 1 capacitor and 3 switches.

Table 3.6: Switching rule: (n is an even number).

State	On	Off
1	Spm, Sgm, Ysm (m=odd number), Ssk, Ypk, Ygk (k=even number), So	Others
2	Ypm, Ygm, Ssm (m=odd number), Ysk, Spk, Sgk (k=even number), Yo	Others

Table 3.7: Switching rule: (n is an odd number).

State	On	Off
1	Spm, Sgm, Ysm (m=odd number), Ssk, Ypk, Ygk (k=even number), Yo	Others
2	Ypm, Ygm, Ssm (m=odd number), Ysk, Spk, Sgk (k=even number), So	Others

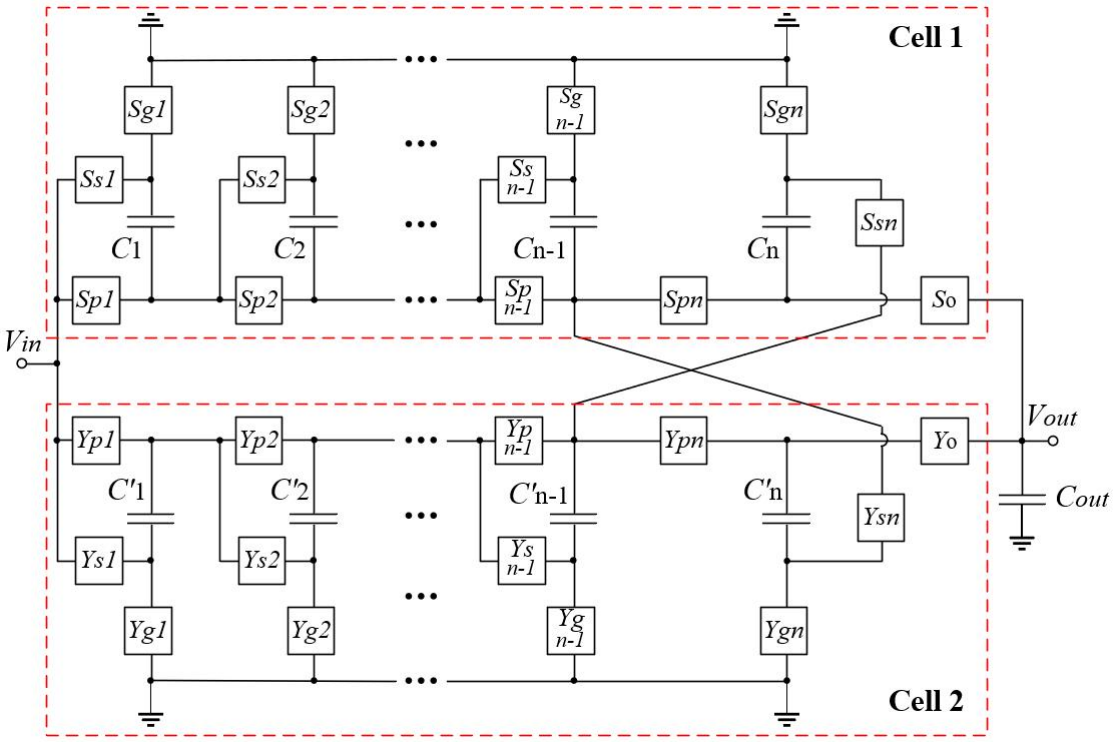
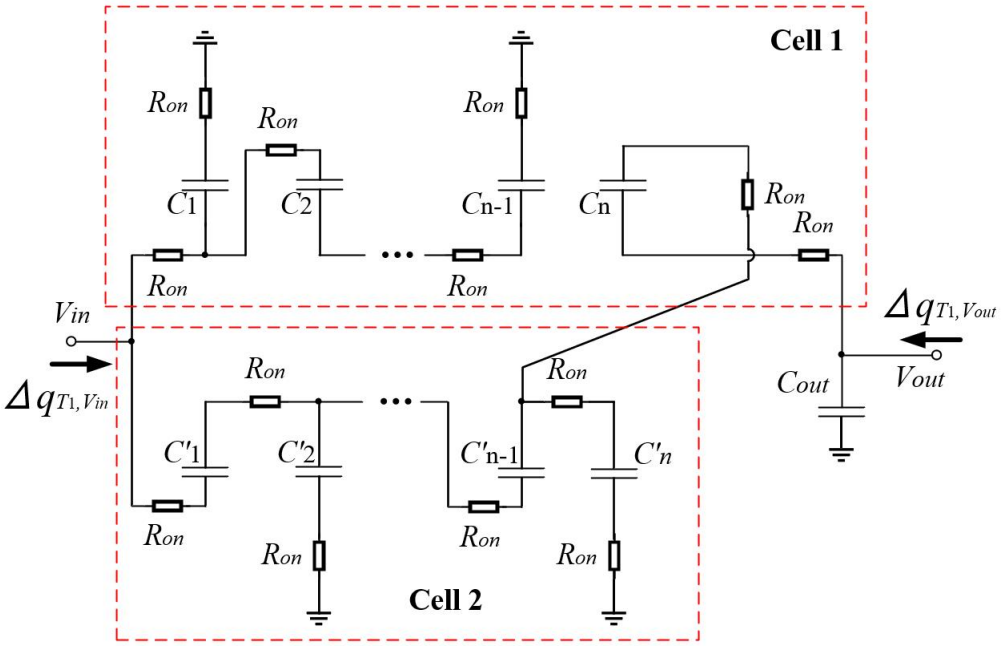
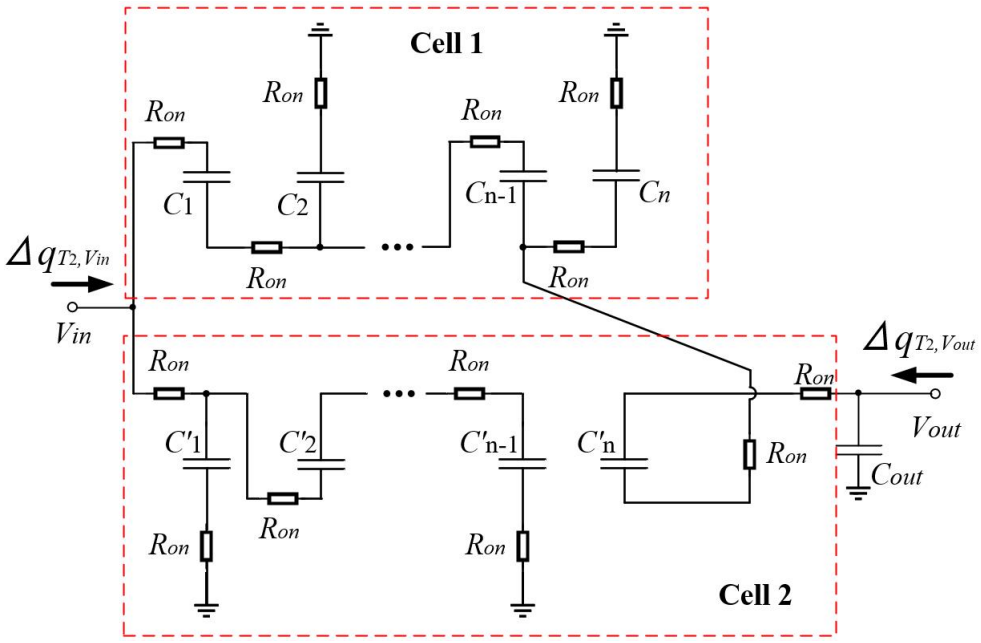


Figure 3.12: Cross-connected Fibonacci topology.



(a) State-1



(b) State-2

Figure 3.13: Instantaneous equivalent circuits of cross-connected Fibonacci topology.

The following analysis is for the conversion ratio of 10. By using KCL, the relations of the electric charge amount of the input, output and capacitors at each operating state are calculated by:

$$\begin{aligned}
\text{State-1}: &\Delta q_{T_1,V_{in}} = -\Delta k^1_{T_1} + \Delta q^1_{T_1} - \Delta q^2_{T_1} \\
&\Delta q^2_{T_1} = -\Delta q^3_{T_1} \\
&\Delta q^4_{T_1} = \Delta k^3_{T_1} + \Delta k^4_{T_1} \\
&\Delta k^3_{T_1} = \Delta k^1_{T_1} + \Delta k^2_{T_1} \\
&\Delta q_{T_1,V_{out}} = \Delta q^4_{T_1} + \Delta q^{out}_{T_1} \\
\text{State-2}: &\Delta q_{T_2,V_{in}} = -\Delta q^1_{T_2} + \Delta k^1_{T_2} - \Delta k^2_{T_2} \\
&\Delta k^2_{T_2} = -\Delta k^3_{T_2} \\
&\Delta k^4_{T_2} = \Delta q^3_{T_2} + \Delta q^4_{T_2} \\
&\Delta q^3_{T_2} = \Delta q^1_{T_2} + \Delta q^2_{T_2} \\
&\Delta q_{T_2,V_{out}} = \Delta k^4_{T_2} + \Delta q^{out}_{T_2}
\end{aligned} \tag{3.62}$$

where $\Delta k^k_{T_i}$ means the electric charges amount of k-th capacitor (C'k) in the cell 2 (n cell) during State-i(i=1,2).

According to the principle of capacitor amp-second balance, the relation of the average input and output current is given by:

$$\langle I_{in} \rangle = -10 \langle I_{out} \rangle , \tag{3.63}$$

where $\Delta q_{V_{in}} = -10\Delta q_{V_{out}}$, $2\Delta q^2_{T_1} = \Delta q_{V_{out}}$ and $\Delta q^j_{T_1} = \Delta k^j_{T_2} = -\Delta q^j_{T_1} = -\Delta k^j_{T_2} (1 \leqq j \leqq n)$.

From Eq. 3.63, the conversion ratio m_{crFibo} is given by:

$$m_{crFibo} = 10. \tag{3.64}$$

The consumed energy by on-resistors of switches during each operating state is calculated as:

$$\begin{aligned}
\text{State-1}: W_{T_1} &= \frac{R_{on}}{T_1} \Big\{ \left(\Delta q^1_{T_1} - \Delta q^2_{T_1}\right)^2 + \left(\Delta q^1_{T_1}\right)^2 + 3\left(\Delta q^2_{T_1}\right)^2 + 2\left(\Delta q^4_{T_1}\right)^2 \\
&\quad + 2\left(\Delta k^1_{T_1}\right)^2 + \left(\Delta k^2_{T_1}\right)^2 + \left(\Delta k^3_{T_1}\right)^2 + 2\left(\Delta k^4_{T_1}\right)^2 \Big\} \\
&= \frac{27 R_{on}}{T_1} \left(\Delta q_{V_{out}}\right)^2 \\
\text{State-2}: W_{T_2} &= W_{T_1}
\end{aligned} \tag{3.65}$$

With the 50% duty ratio, the total consumed energy during one operating cycle is obtained as:

$$W_T = \sum_{i=1}^{2} W_{T_i} = 2W_{T_1} = \frac{108R_{on}}{T}\left(\Delta q_{T_{V_{out}}}\right)^2. \tag{3.66}$$

Comparing Eqs. 3.66 and 2.14, the R_{SC} of the cross-connected Fibonacci topology is given by:

$$R_{SC} = 108R_{on}. \tag{3.67}$$

The K-matrix of the topology can be expressed by:

$$\begin{bmatrix} \langle V_{in} \rangle \\ \langle I_{in} \rangle \end{bmatrix} = \begin{bmatrix} \frac{1}{10} & 0 \\ 0 & 10 \end{bmatrix} \begin{bmatrix} 1 & 108R_{on} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \langle V_{out} \rangle \\ -\langle I_{out} \rangle \end{bmatrix}. \tag{3.68}$$

From above steps, the maximum efficiency and output voltage of the cross-connected Fibonacci topology is calculated as:

$$\eta_{max} = \frac{R_L}{R_L + R_{SC}} = \frac{R_L}{R_L + 108R_{on}}. \tag{3.69}$$

$$V_{out\_max} = \left(\frac{R_L}{R_L + 108R_{on}}\right) V_{in}. \tag{3.70}$$

Using the same analysis way as the case of 10 conversion ratio, the R_{SC} of the cross-connected Fibonacci topology with the conversion ratios (4,6,10 and 16) can be calculated as shown in Tab. 3.8.

Table 3.8: R_{SC} of cross-connected Fibonacci topology at different conversion ratios

m_{crFibo}	R_{SC}
4	$16R_{on}$
6	$40R_{on}$
10	$108R_{on}$
16	$280R_{on}$

3.3 Comparing Topologies

The core and modified topologies are analyzed based on the four-terminal equivalent circuit model in Section 3.1 and 3.2. According to the modeling, R_{SC} values of the topologies affect the performances of them. In this section, the topologies are simulated to measure their power efficiencies and output ripple voltages, and then compared at different conversion ratios from 2 to 20 by the theoretical analysis and simulations.

3.3.1 Comparing Core Topologies

Figure 3.14 shows R_{SC} values of the three core topologies at different conversion ratios. According to the theoretical analysis, the smaller R_{SC} a topology has, the higher power efficiency it has. The simulation results as shown in Figure 3.15 improve the validity of the parameter R_{SC} with negligible errors. In Figure 3.15, the power efficiency based on the FE model is calculated by using Eq. 3.10, 3.20 and Table 3.5. The simulation is implemented with the condition in Table 3.9. When the Fibonacci topology is operated by three operating states, the parameters as follows: $T = 1.5\mu s$ and $D = \frac{1}{3}$.

The Fibonacci topology has the lowest power efficiency over the conversion ratio of 9 except for 13. The Dickson topology has the highest power efficiency among three topologies at every conversion ratio. However, the number of circuit components in the Dickson topology is approcimately three times bigger than the Fibonacci topology at the conversion ratio 20 as shown in Figure 3.16. The Fibonacci topology has the smallest number of circuit components through all conversion ratios in the sense that it generates various kinds of output voltages with the restricted number of circuit components. However, when the Fibonacci topology produces the stepped-up voltages of the non-Fibonacci numbered conversion ratios, three states (three-phase) operation is required. This operation causes the higher output ripple voltage as shown in Figure 3.17.

The comparison in this section can provide a standard of selecting a core topology of SC DC-DC converters when the selection issues are its power efficiency, circuit size and output ripple voltage.

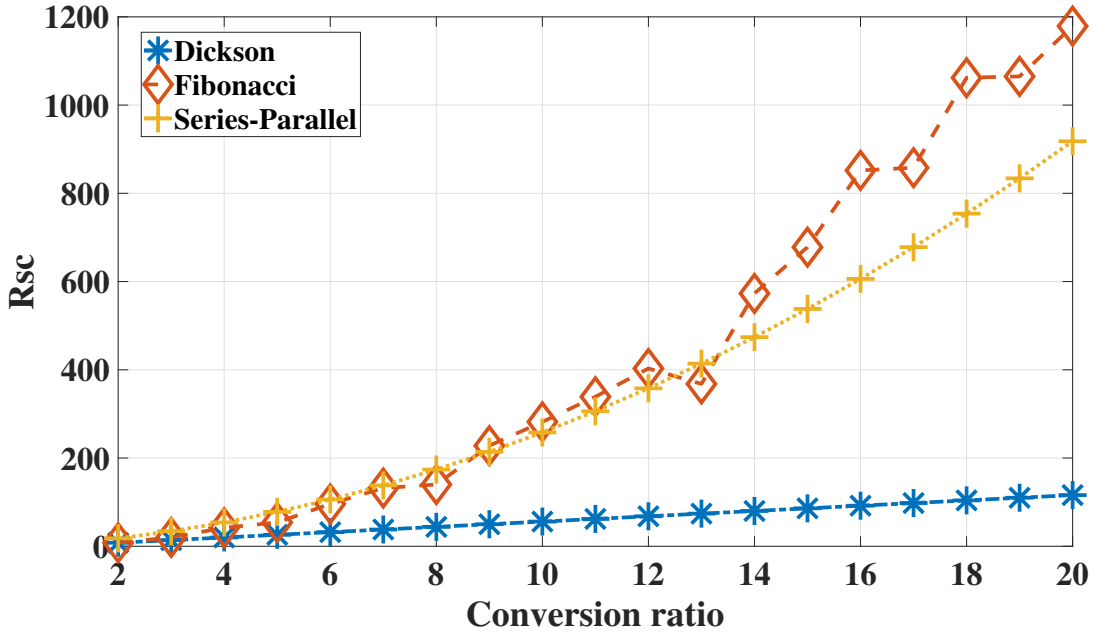
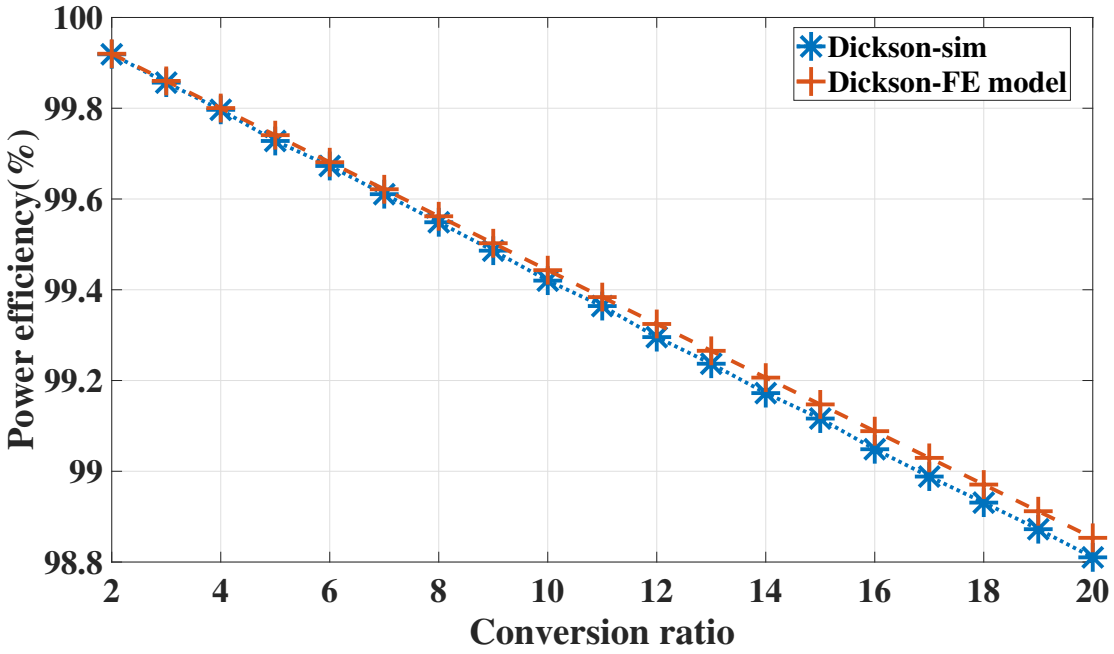


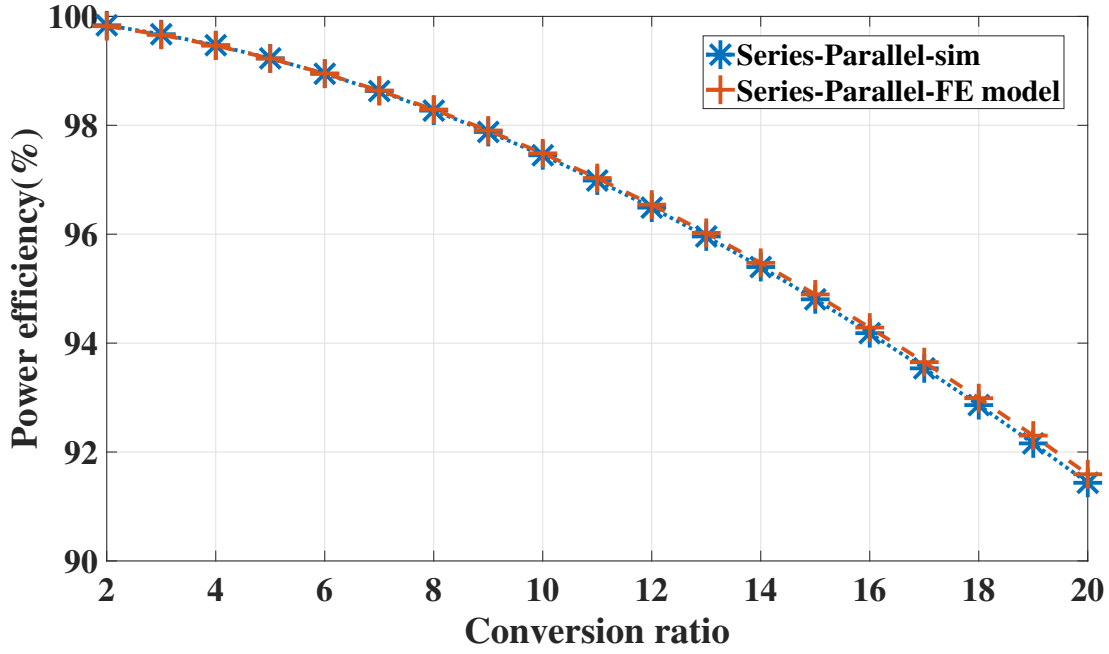
Figure 3.14: R_{SC} vs. conversion ratio.

Table 3.9: Simulation condition.

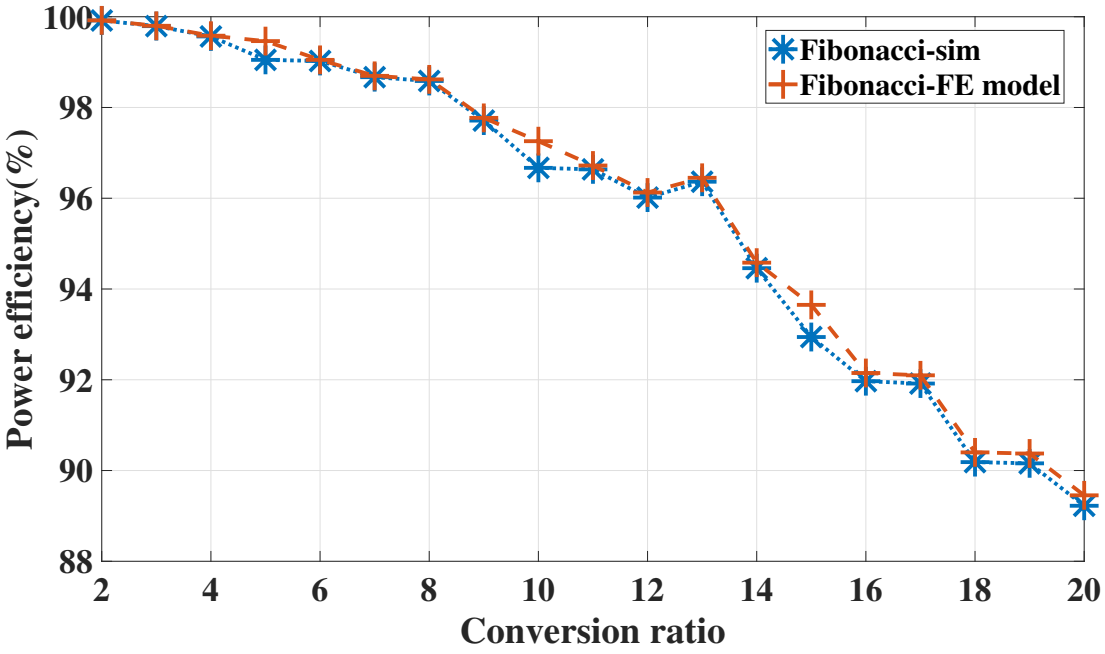
Parameter	Values
R_{on}	0.1Ω
R_L	1kΩ
T	1μs
C	10μF
D	0.5
V_{in}	10V



(a) Dickson topology

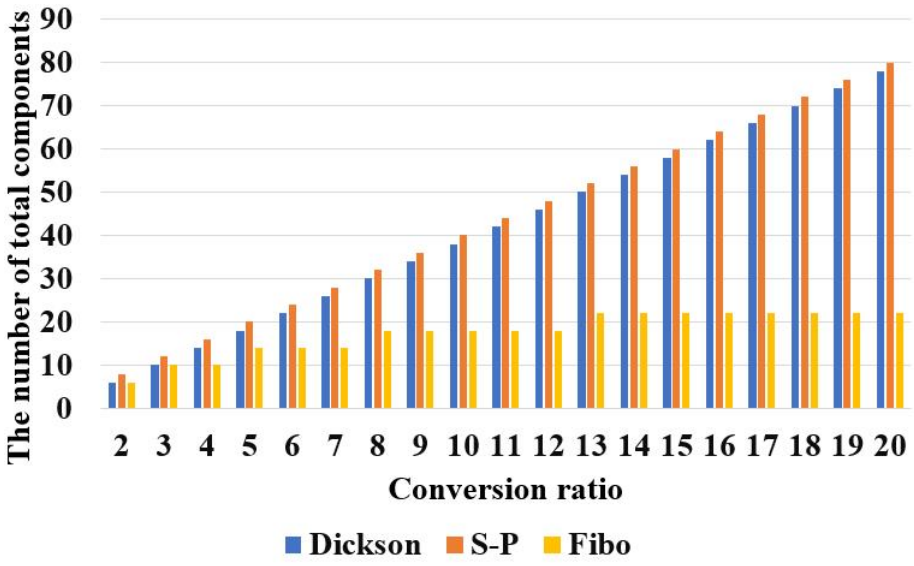


(b) Series-parallel topology

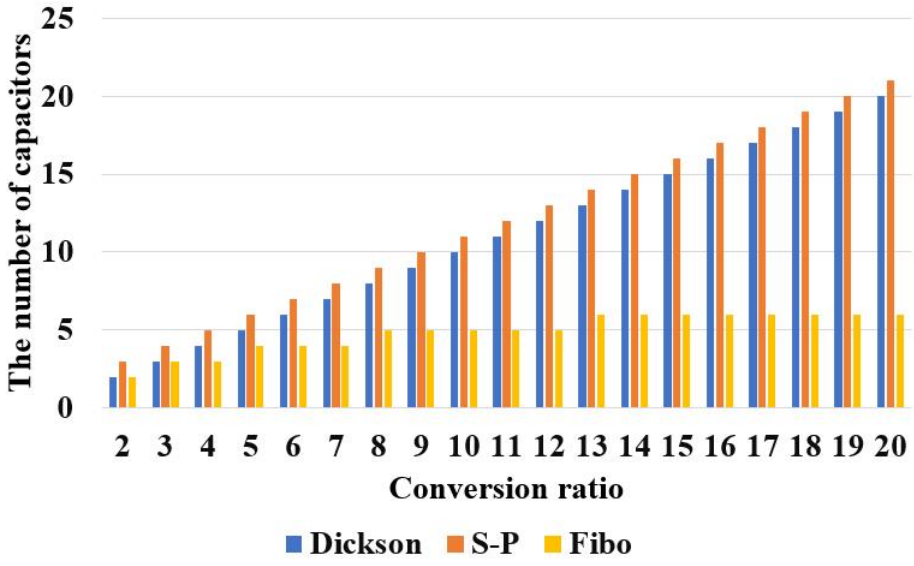


(c) Fibonacci topology

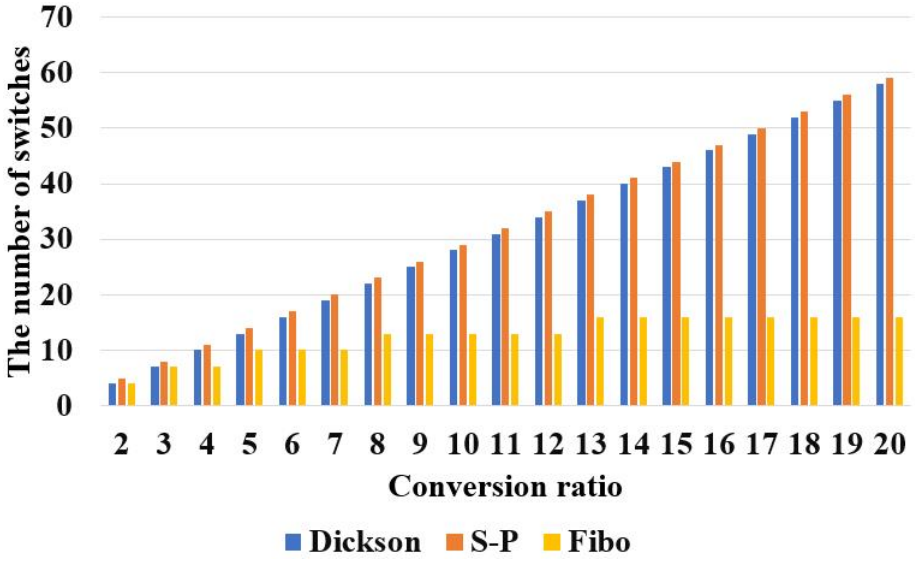
Figure 3.15: Comparison of FE model with simulation at different conversion ratios (core topologies).



(a) The number of total components



(b) The number of capacitors



(c) The number of switches

Figure 3.16: The number of circuit components of three topologies: S-P is for series-parallel and Fibo is for Fibonacci.

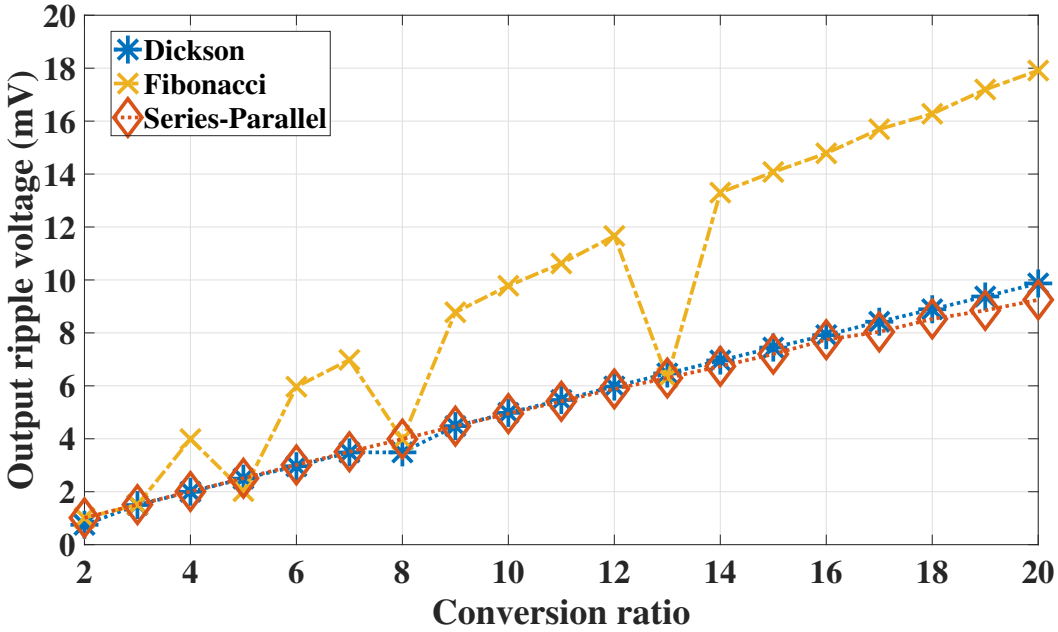


Figure 3.17: Simulated output ripple voltages of three core topologies.

3.3.2 Comparing Modified Topologies

SCVM vs. Series-Paraell: In this comparison, the SCVM topology has 11 kinds of conversion ratios: 4, 6, 8, 9, 10, 12, 14, 15, 16, 18, 20. The limited conversion ratios is attributed to the fact that with a prime numbered conversion ratio (2, 3, 5, ...), the SCVM topology turns out to be the same as the series-parallel topology. Table 3.10 shows the number of capacitors in each cell of the SCVM topology.

The power efficiency of the SCVM topology is worse than the series-parallel topology throughout all conversion ratios according to comparing R_{SC} of two topologies as shown in Figure 3.18. The validity of the R_{SC} of the SCVM topology is verified with neglectable errors by the simulation as shown in Figure 3.19. The power efficiency from the FE model in Figure 3.19 is derived by using Eq. 3.50. The simulation is conducted with the condition on Table 3.9 and 3.10.

Table 3.10: The number of capacitors of SCVM topology in each cell

Conversion ratios	m cell	n cell
4	2	2
6	3	2
8	4	2
9	3	3
10	5	2
12	6	2
14	7	2
15	5	3
16	8	2
18	9	2
20	10	2

At the same conversion ratio, the difference of the output ripple voltage between two topologies has almost zero as shown in Figure 3.20.

While having the restricted conversion ratios and worse power efficiency, the SCVM topology can reduce the number of circuit components as shown in Figure 3.24. The SCVM topology can be a solution when a small size topology with a

large load value is needed because the larger load value can weaken the impact of R_{SC} on the power efficiency.

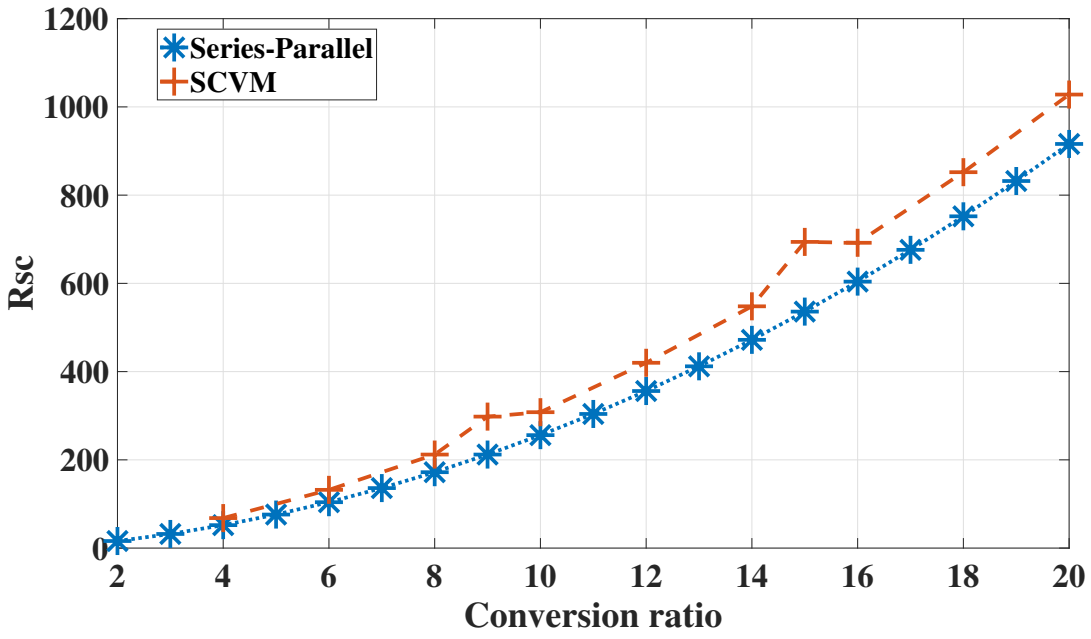


Figure 3.18: R_{SC} of SCVM and series-parallel topology at different conversion ratios.

Symmetrical Dickson vs. Normal Dickson: To compare the symmetrical and normal Dickson topologies, the symmetrical one is simulated with the condition on Table. 3.9. The error between calculated by Eq. 3.60 and simulated power efficiencies is trivial as shown in Figure 3.22.

The R_{SC} of the symmetrical Dickson topology is higher than that of the normal Dickson topology at every conversion ratio as shown in Figure 3.21. In other words, the power efficiency of the symmetrical one is improved by the symmetrical structure. Despite the benefit of improved power efficiency, the circuit size of the symmetrical one becomes bulkier than the normal one as shown in Figure 3.24.

Figure 3.23 presents the output ripple voltages of two topologies at different conversion ratios. The output ripple voltages of the symmetrical Dickson topology are reduced by 30 times on average, compared to that of the normal Dickson topology.

If the circuit size or the number of components is not a critical issue, the symmetrical Dickson topology can improve the power efficiency of a target system.

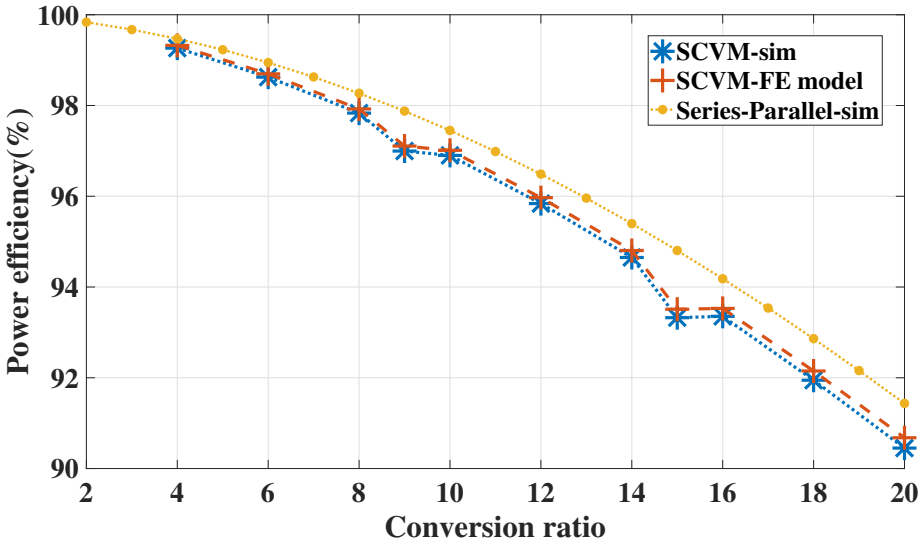


Figure 3.19: Comparison of FE model with simulation at different conversion ratios (SCVM topology).

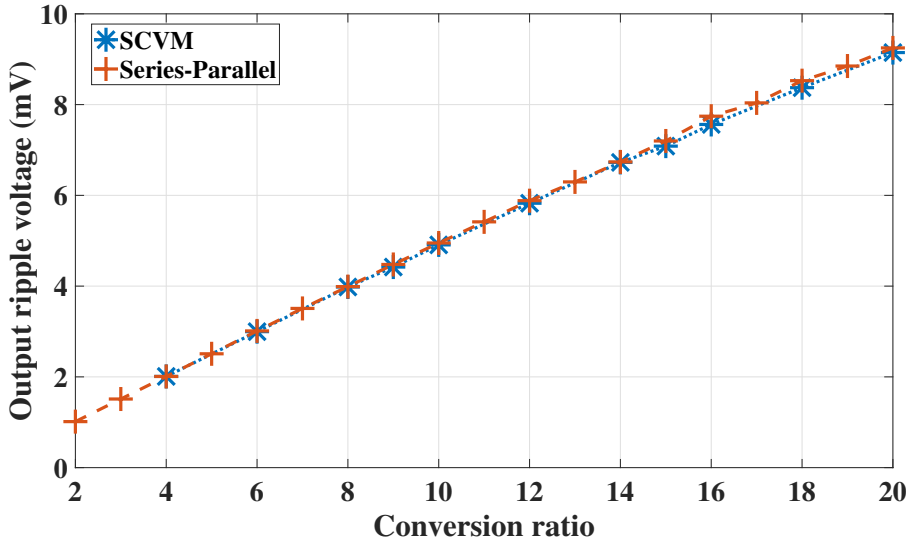


Figure 3.20: Output ripple voltages of SCVM and series-parallel topology at different conversion ratios.

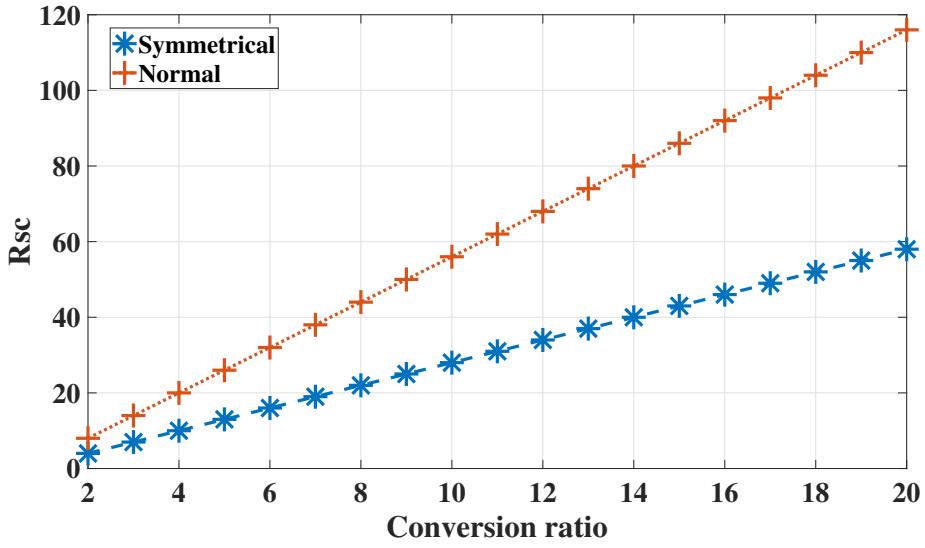


Figure 3.21: R_{SC} of symmetrical and normal Dickson topology at different conversion ratios.

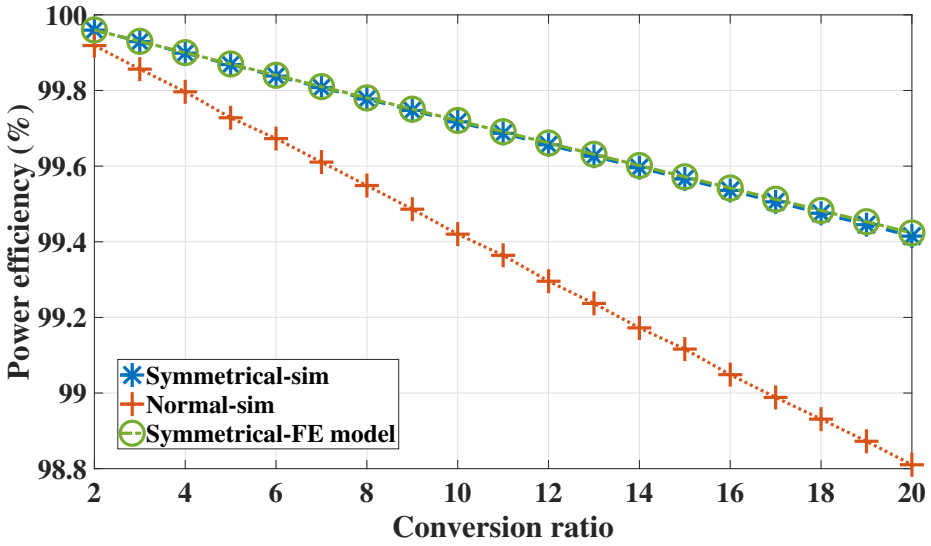


Figure 3.22: Comparison of FE model with simulation at different conversion ratios (symmetrical Dickson topology).

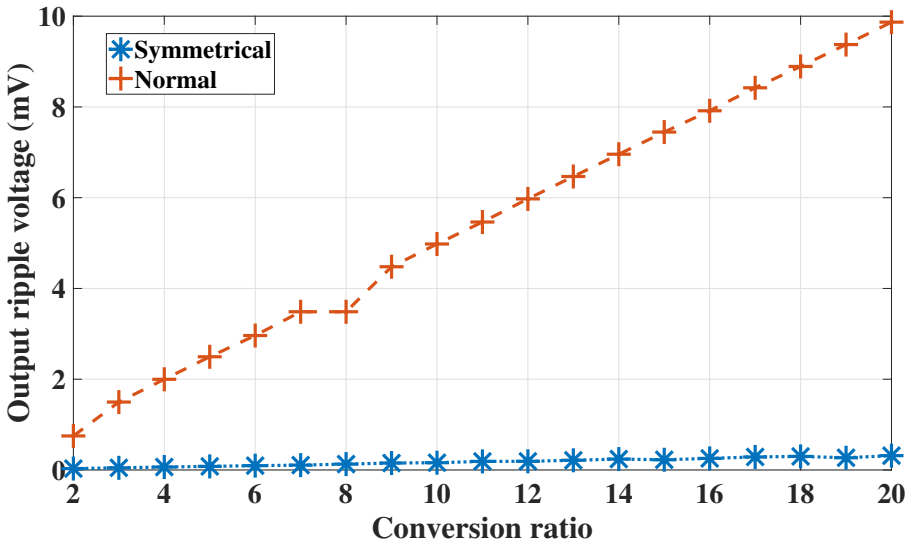


Figure 3.23: Output ripple voltages of symmetrical and normal Dickson topology at different conversion ratios.

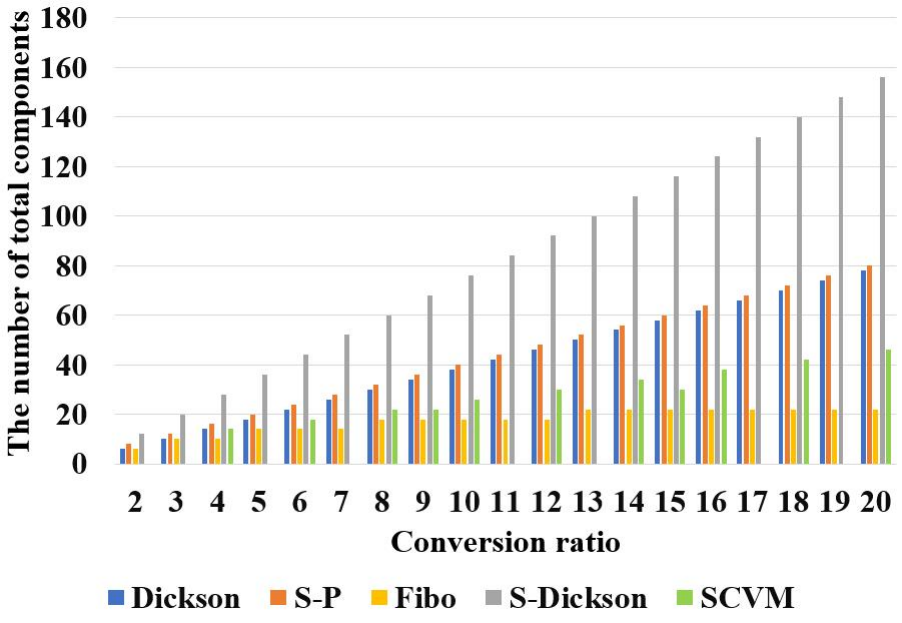
Cross-connected Fibonacci vs. Normal Fibonacci: The cross-connected Fibonacci topology is simulated with the condition on Table. 3.9. Figure 3.27 indicates the negligible errors between the calculated and simulated power efficiencies at the different conversion ratios.

The R_{SC} of the cross-connected Fibonacci topology is higher than the normal one at each conversion ratio (4, 6, 10 and 16) as shown in Figure 3.25, which means the cross-connected one has higher power efficiency than the normal one. However, the cross-connected topology is required to have almost twice as many circuit components as the normal one has. Furthermore, the cross-connected topology has the limited conversion ratios (even Fibonacci numbers over 2).

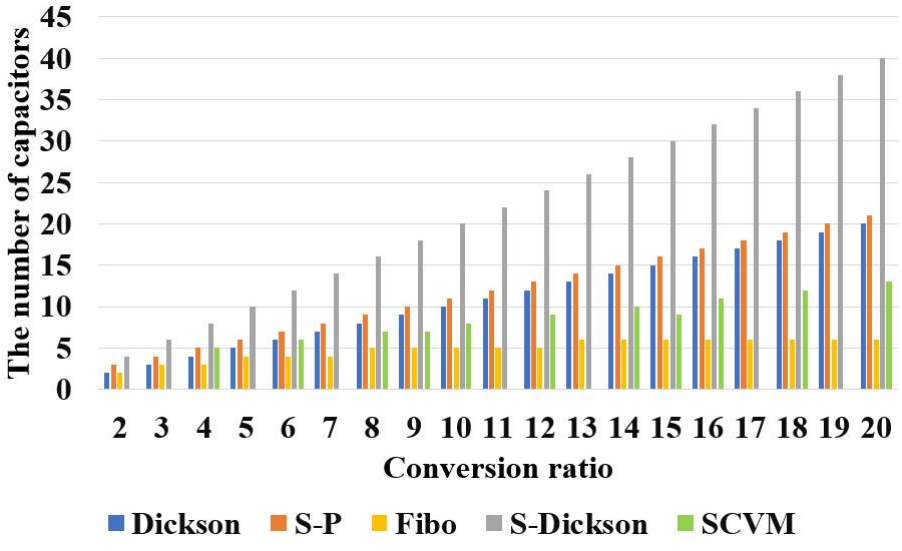
Comparing with the normal Fibonacci topology, the circuit size of the cross-connected Fibonacci one is bigger than that of the normal one as shown in Figure 3.28.

The output ripple voltage of the cross-connected topology improves up to 60 times at the conversion ratio of 6 as described in Figure 3.27. This improvement is caused by the feature of the symmetric structure.

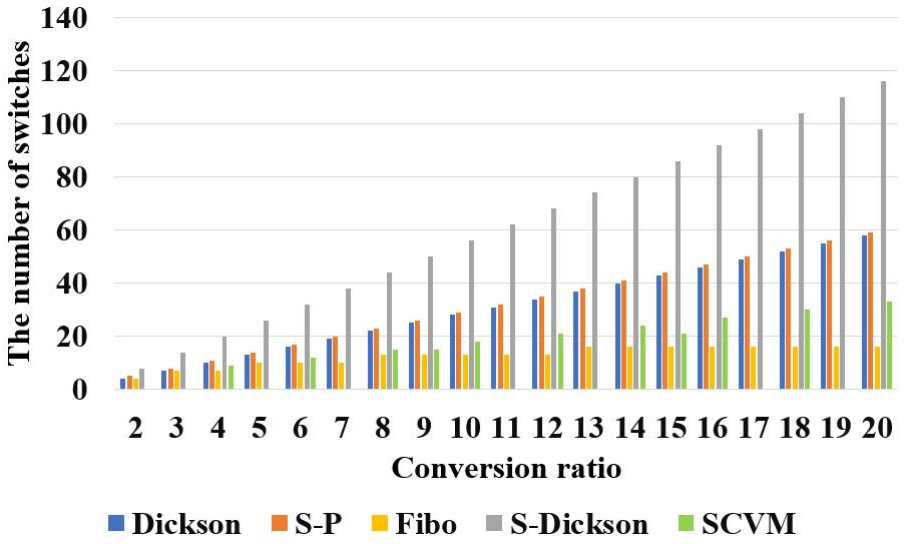
When an efficient SC DC-DC topology is needed with the low output ripple voltage and a specific conversion ratio such as even Fibonacci number greater than 2, the cross-connected Fibonacci topology can be worth consideration.



(a) The number of total components (5 topolgoies)



(b) The number of capacitors (5 topolgoies)



(c) The number of switches (5 topolgoies)

Figure 3.24: The number of circuit components of core and modified topologies

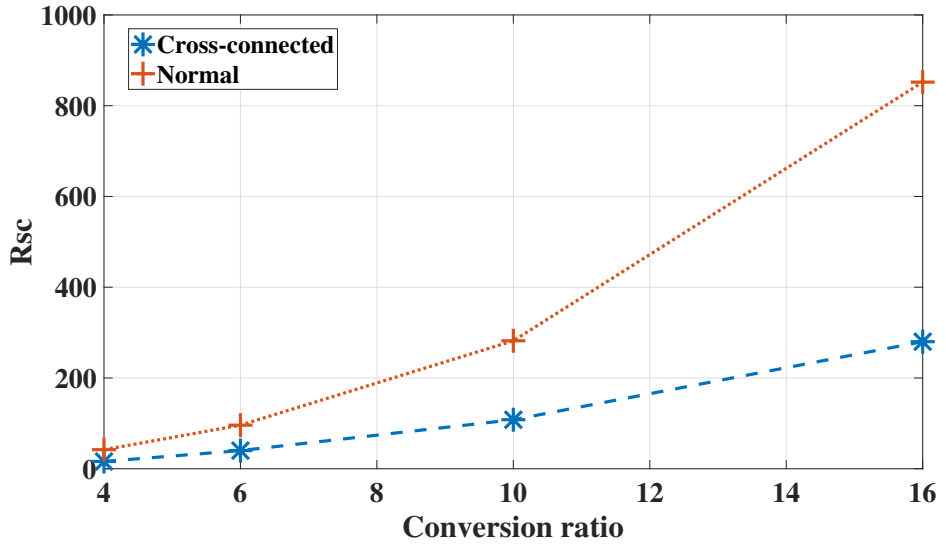


Figure 3.25: Comparison of R_{SC} of Fibonacci topologies.

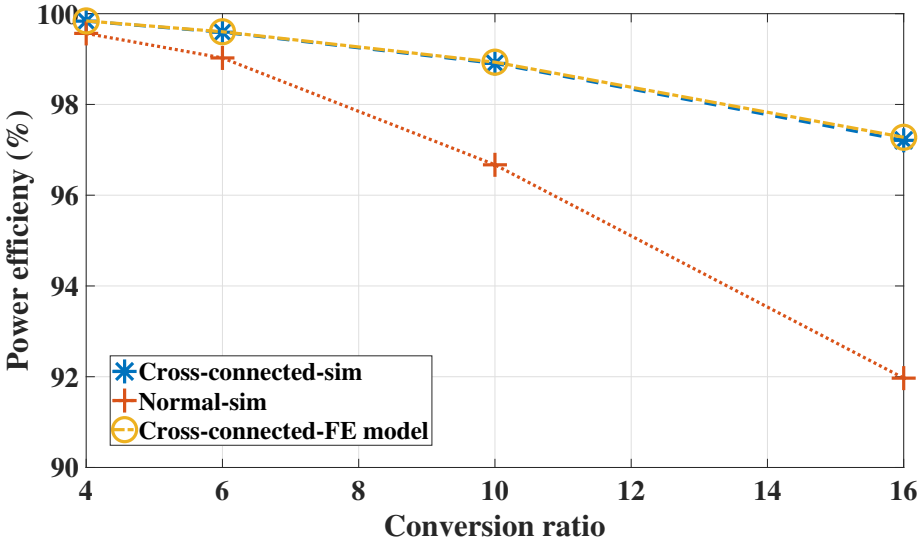


Figure 3.26: Comparison of power efficiencies of Fibonacci topologies.

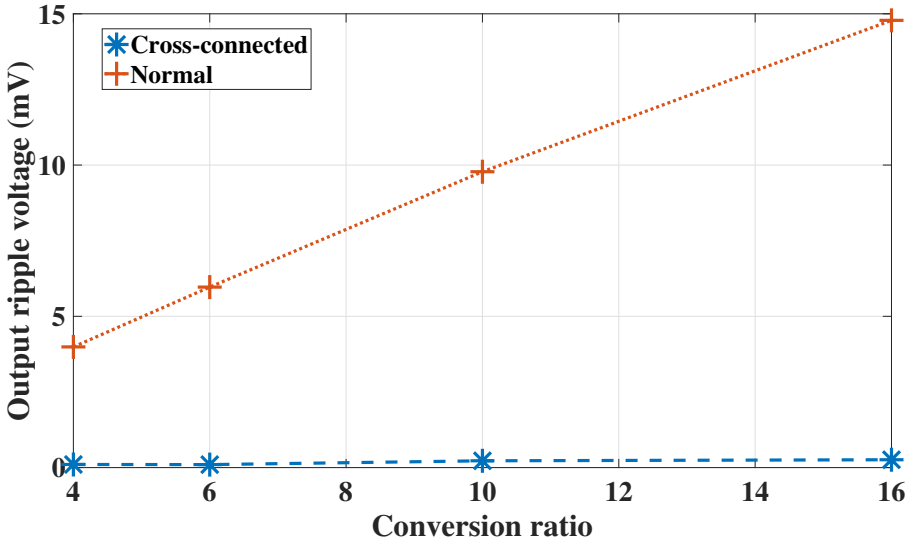
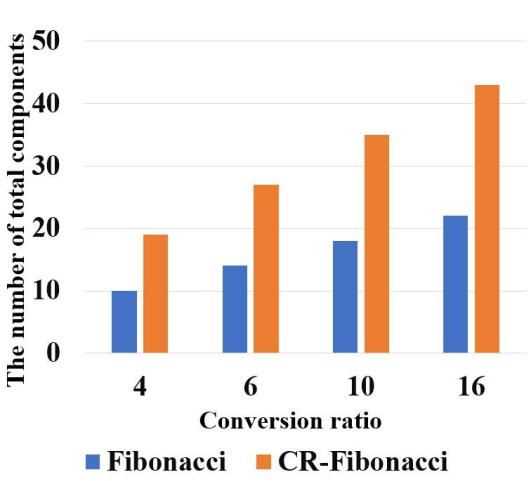
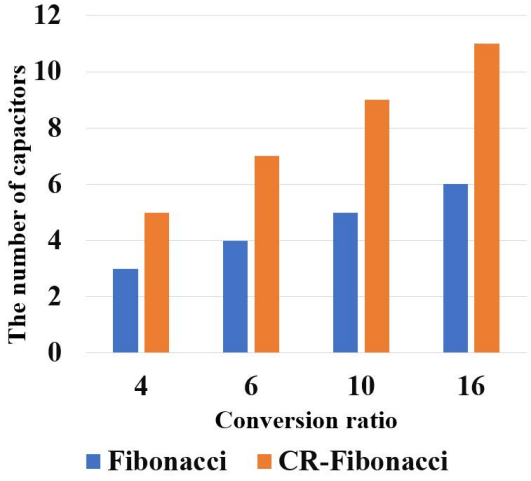


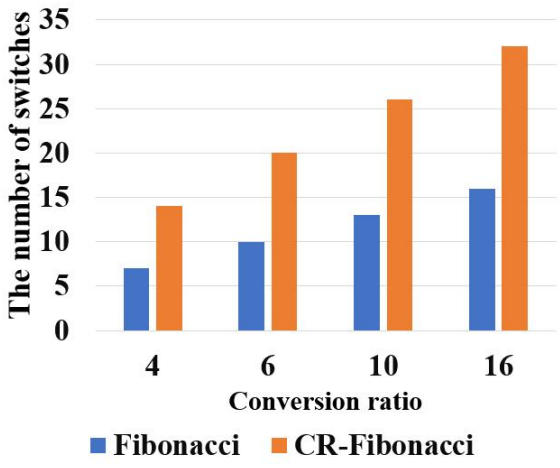
Figure 3.27: Comparison of output ripple voltages of Fibonacci topologies.



(a) The number of total components (Fibonacci topolgoies)



(b) The number of capacitors (Fibonacci topolgoies)



(c) The number of switches (Fibonacci topolgoies)

Figure 3.28: The number of circuit components of Fibonacci topologies

Chapter 4

Suggestion of New Topologies

4.1 Cross-connected Dickson Topology

Figure 4.1 depicts a new Dickson topology. The new topology is named cross-connected Dickson topology in the sense that n-th capacitors in each cell are linked to the (n-1)-th capacitors, respectively. The cross-connected Dickson topology consists of $(2n + 1)$ capacitors, one output capacitor and $(6n + 2)$ switches. These switches ($S1$ and $S2$) are oppositely turned on and off, by which the proposed topology has two instantaneous equivalent circuits as shown in Figure 4.2. By the cross connected structure, the output voltage of the proposed topology is 2 times higher than the symmetrical Dickson topology when the number of circuit components in two topologies are the same. The output ripple voltage of the proposed one is lower than the normal Dickson topology because of the symmetrical structure.

4.2 Enhanced Cross-connected Fibonacci Topology

Although the new topology is suggested in the before subsection, there is a room for designing an SC DC-DC topology with the smaller number of circuit components as well as its higher conversion ratio at the similar number of them.

The newly suggested topology is the enhanced cross-connected Fibonacci topology as shown in Figure 4.3. The new topology is based on the normal and cross-connected Fibonacci topology. The charging operation is similar to the Fibonacci topology in the sense that charged capacitors in previous state charge the capacitors in the next stage, where a stage is defined as a block of 1 capacitor and 3 switches

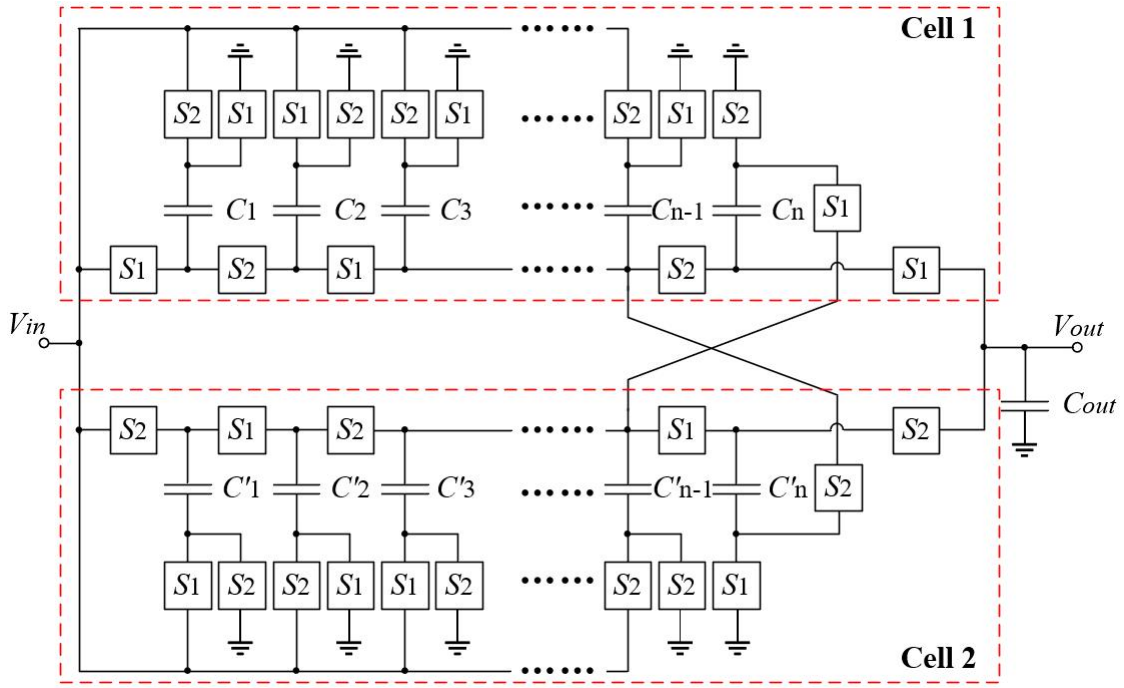
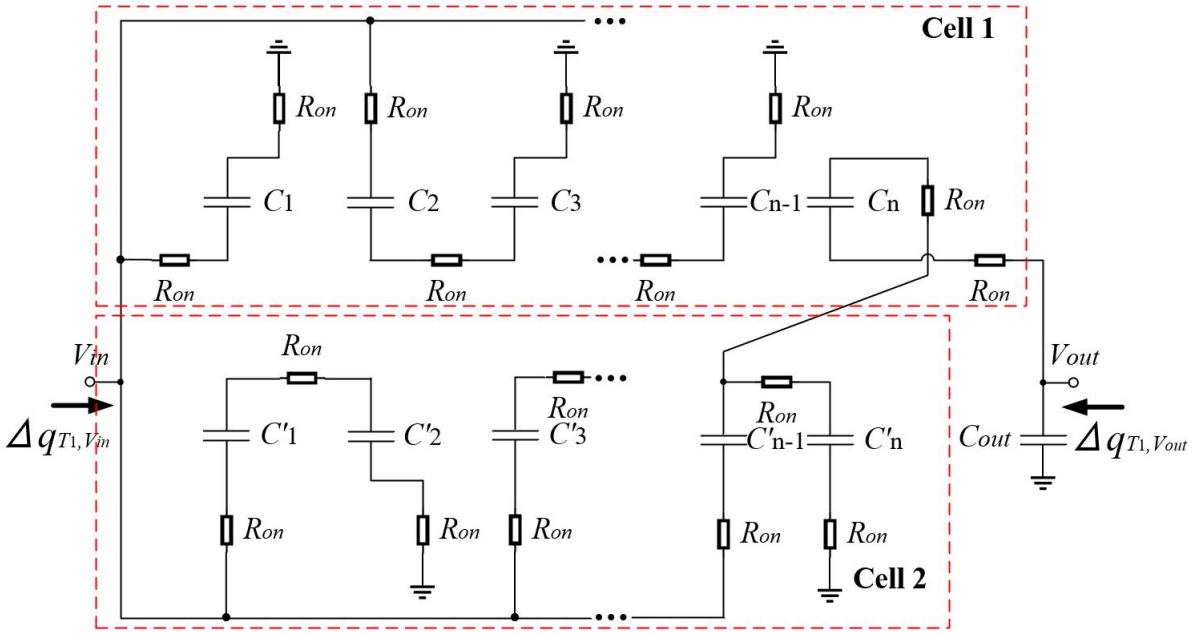


Figure 4.1: Cross-connected Dickson topology.

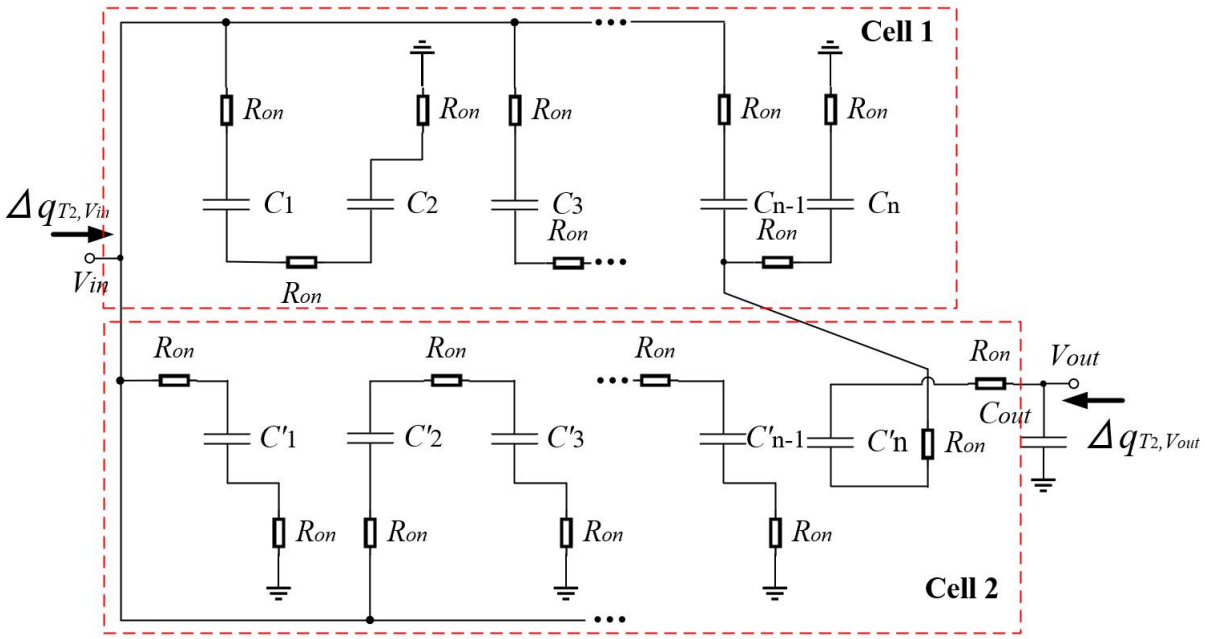
in the converter cell. More strictly, (k-1)-th capacitor charges k-th capacitor, where $2 \leqq k \leqq n$.

Unlike the cross-connected Fibonacci topology in section 3.2.3, the distinguished structural feature is that switches Ssk and Ysk ($2 \leqq k \leqq n$) are cross-connected to each of the opposite cell. By the cross-connection in all stages, the proposed topology can generate 2^n times the input voltage V_{in}.

The switches in the proposed topology are operated by the same switching rule of the cross-connected Fibonacci topology in Table 3.6 and Table 3.7. From this switching, the proposed topology has two instantaneous equivalent circuits as shown in Figure 4.4.



(a) State-1



(b) State-2

Figure 4.2: Instantaneous equivalent circuits of cross-connected Dickson topology.

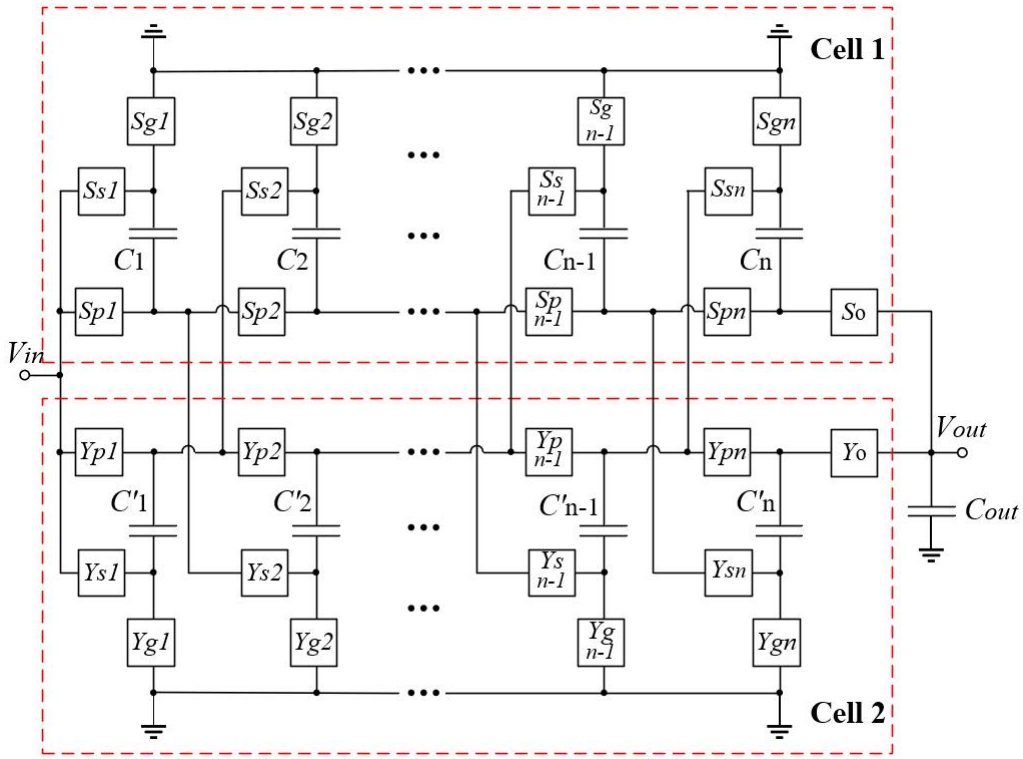
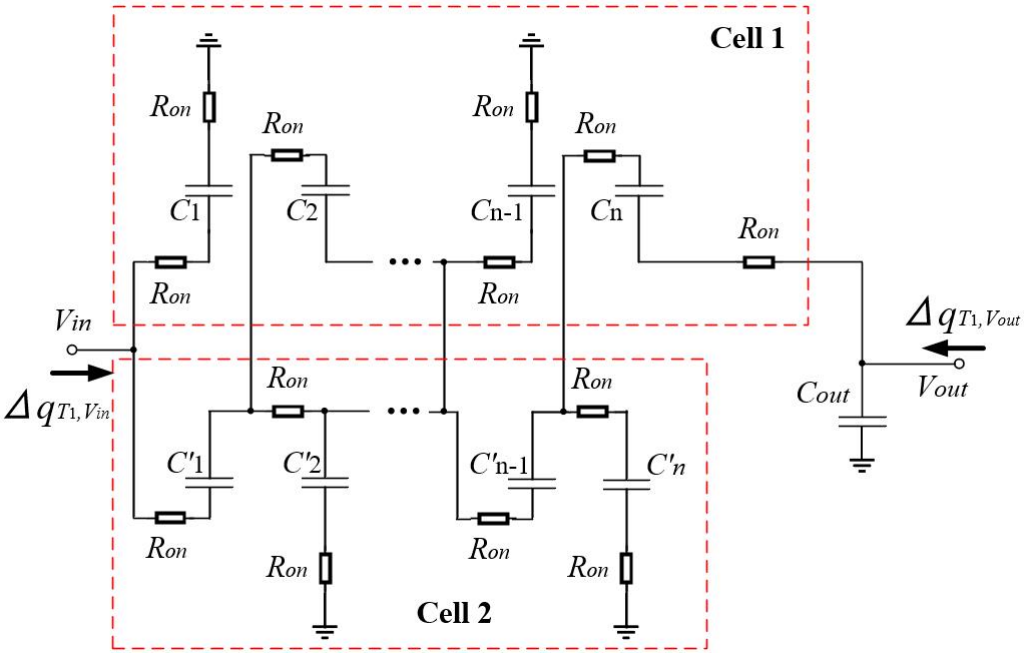
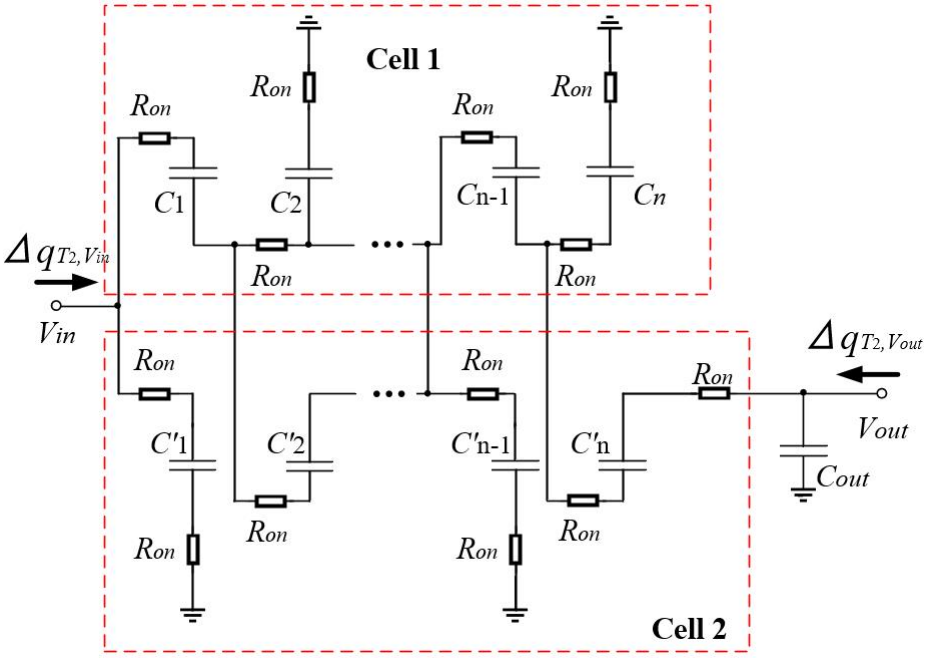


Figure 4.3: Enhanced cross-connected Fibonacci topology.



(a) State-1



(b) State-2

Figure 4.4: Instantaneous equivalent circuits of enhanced cross-connected Fibonacci topology.

Chapter 5

Analysis of New Topologies

This section performs the analysis of the suggested topologies based on the FE model. Then, the proposed topologies are compared with their family topologies to evaluate their performance. Finally, the feasibilities of the suggested topologies are verified by building them on a breadboard.

5.1 Cross-connected Dickson Topology

5.1.1 Theoretical Analysis

The proposed topology is analyzed by the FE model. In a steady state, the charge amounts of all capacitors satisfy the following equation according to the principle of capacitor amp-second balance and the symmetrical structure.

$$\begin{aligned} &\Delta q^k_{T_1} + \Delta q^k_{T_2} = 0, \\ &\Delta k^k_{T_1} + \Delta k^k_{T_2} = 0, \\ &\Delta q^k_{T_1} = \Delta k^k_{T_2} = -\Delta q^k_{T_2} = -\Delta k^k_{T_1}, \end{aligned} \tag{5.1}$$

where $(1 \leqq k \leqq n)$ and $\Delta q^k_{T_i}$ and $\Delta k^k_{T_i}$ is the k-th capacitor of the cell 1 and 2 in state-i $(i = 1, 2)$, respectively.

By setting the duty ratio D to 50%, T can be written as:

$$T = \sum_{i=1}^{2} T_i \quad \text{and} \quad T_1 = T_2 = \frac{T}{2}, \tag{5.2}$$

where $T_1 = (1 - D)T$ and $T_2 = DT$.

By using KCL, the relations of the electric charge amount of the input, output and capacitors at each operating state are calculated by:

$$\begin{aligned}
\text{State-1 :}&\Delta q_{T_1,V_{in}} = \Delta q_{T_1}^1 - \Delta q_{T_1}^2 - \Delta q_{T_1}^4 - \cdots - \Delta q_{T_1}^{n-2} \\
&\qquad + \Delta k_{T_1}^2 + \Delta k_{T_1}^4 + \Delta k_{T_1}^6 + \cdots + \Delta k_{T_1}^{n-2} + \Delta k_{T_1}^{n-1} \\
&\Delta q_{T_1}^n = \Delta k_{T_1}^n + \Delta k_{T_1}^{n-1} \\
&\Delta q_{T_1,V_{out}} = \Delta q_{T_1}^n + \Delta q_{T_1}^{out} \\
\text{State-2 :}&\Delta q_{T_2,V_{in}} = \Delta k_{T_2}^1 - \Delta k_{T_2}^2 - \Delta k_{T_2}^4 - \cdots - \Delta k_{T_2}^{n-2} \\
&\qquad + \Delta q_{T_2}^2 + \Delta q_{T_2}^4 + \Delta q_{T_2}^6 + \cdots + \Delta q_{T_2}^{n-2} + \Delta q_{T_2}^{n-1} \\
&\Delta k_{T_2}^n = \Delta q_{T_2}^n + \Delta q_{T_2}^{n-1} \\
&\Delta q_{T_2,V_{out}} = \Delta q_{T_1}^n + \Delta q_{T_2}^{out}.
\end{aligned} \tag{5.3}$$

Substituion of Eq.5.1 into Eq.5.3 leads to

$$\begin{aligned}
\Delta q_{V_{out}} &= \Delta q_{T_1,V_{out}} + \Delta q_{T_2,V_{out}} \\
&= 2\Delta q_{T_1}^n \\
\Delta k_{T_1}^{n-1} &= \Delta q_{T_1}^n - \Delta k_{T_1}^n \\
&= 2\Delta q_{T_1}^n \\
&= \Delta q_{V_{out}}.
\end{aligned} \tag{5.4}$$

From Eqs. 5.1-5.4, the relation of the average input and output current is given by:

$$\langle I_{in} \rangle = -2n \langle I_{out} \rangle , \tag{5.5}$$

where $\Delta q_{V_{in}} = -2n\Delta q_{V_{out}}$.

From Eq. 5.5, the conversion ratio $m_{crossDickson}$ is given by:

$$m_{crossDickson} = 2n. \tag{5.6}$$

The consumed energy by on-resistors of switches during each operating state is calculated as:

$$\begin{aligned}
\text{State-1 :}W_{T_1} &= \frac{2R_{on}}{T_1}\left(\Delta q_{T_1}^1\right)^2 + \frac{3R_{on}}{T_1}\left(\Delta q_{T_1}^2\right)^2 + \frac{3R_{on}}{T_1}\left(\Delta q_{T_1}^4\right)^2 + \cdots \\
&\quad + \frac{R_{on}}{T_1}\left(\Delta q_{T_1}^n\right)^2 + \frac{3R_{on}}{T_1}\left(\Delta k_{T_1}^2\right)^2 + \frac{3R_{on}}{T_1}\left(\Delta k_{T_1}^4\right)^2 + \cdots \\
&\quad + \frac{R_{on}}{T_1}\left(\Delta k_{T_1}^n\right)^2 + \frac{2R_{on}}{T_1}\left(\Delta k_{T_1}^n\right)^2 \\
&= \frac{(3n-2)\,R_{on}}{T_1}\left(\Delta q_{V_{out}}\right)^2
\end{aligned} \tag{5.7}$$

State-2 :$W_{T_2} = W_{T_1}$

With the 50% duty ratio, the total consumed energy during one operating cycle is obtained as:

$$\begin{aligned} W_T &= \sum_{i=1}^{2} W_{T_i} = 2W_{T_1} = \frac{(6n-4)\,R_{on}}{T_1}\left(\Delta q_{T_{V_{out}}}\right)^2 \\ &= \frac{(12n-8)R_{on}}{T}\left(\Delta q_{T_{V_{out}}}\right)^2. \end{aligned} \tag{5.8}$$

Comparing Eqs. 3.57 and 2.14, the R_{SC} of the cross-connected Dickson topology is given by:

$$R_{SC} = (12n-8)\,R_{on}. \tag{5.9}$$

The K-matrix of the proposed topology can be expressed by:

$$\begin{bmatrix} \langle V_{in} \rangle \\ \langle I_{in} \rangle \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & (12n-8)\,R_{on} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \langle V_{out} \rangle \\ -\langle I_{out} \rangle \end{bmatrix}. \tag{5.10}$$

From above steps, the maximum efficiency and output voltage of the cross-connected Dickson topology is calculated as:

$$\eta_{max} = \frac{R_L}{R_L + R_{SC}} = \frac{R_L}{R_L + (12n-8)\,R_{on}}. \tag{5.11}$$

$$V_{out\_max} = \left\{ \frac{R_L}{R_L + (12n-8)\,R_{on}} \right\} V_{in}. \tag{5.12}$$

5.1.2 Simulation and Comparison

In this subsection, the proposed topology is compared with the normal and symmetrical Dickson topologies.

Figure 5.1 depicts the R_{SC} of three Dickson topologies at the different conversion ratios from 4 to 20. By the structure characteristic of the proposed topology, it has $2n$ ($n \geqq 2$) conversion ratio. Through all conversion ratios, R_{SC} values of the proposed topology are smaller than those of the normal one but higher than those of the symmetrical one. In other words, the power efficiency of the proposed topology is middle level among three Dickson topologies. Figure 5.2 shows negligible errors between the calculated and simulated power efficiencies of the proposed topologies. The simulation is carried out with the condition on Table 3.9. Additionally, while the power efficiency of the proposed topology is the second best among three topologies, that of the proposed one is higher than that of other topologies such as the series-parallel topology or normal and cross-connected Fibonacci topology.

The output ripple voltages of three topologies are measured by the simulation as shown in Figure 5.3. The output ripple voltage of the proposed topology is almost the same as that of the symmetrical one. Because the proposed topology also includes the symmetrical structure, the proposed one can decrease the output ripple voltage, comparing to the normal one.

The number of required circuit components for three Dickson topologies is shown in Figure 5.4. The proposed topology can reduce the number of circuit components in comparison with the symmetric one at the same conversion ratio. Comparing the normal Dickson topology, the proposed one has 1 capacitor and 6 switches more at all conversion ratios.

Although the cross-connected Dickson topology has limited conversion ratios, it can be a solution when the following conditions are the issues: small size, low output ripple and high power efficiency.

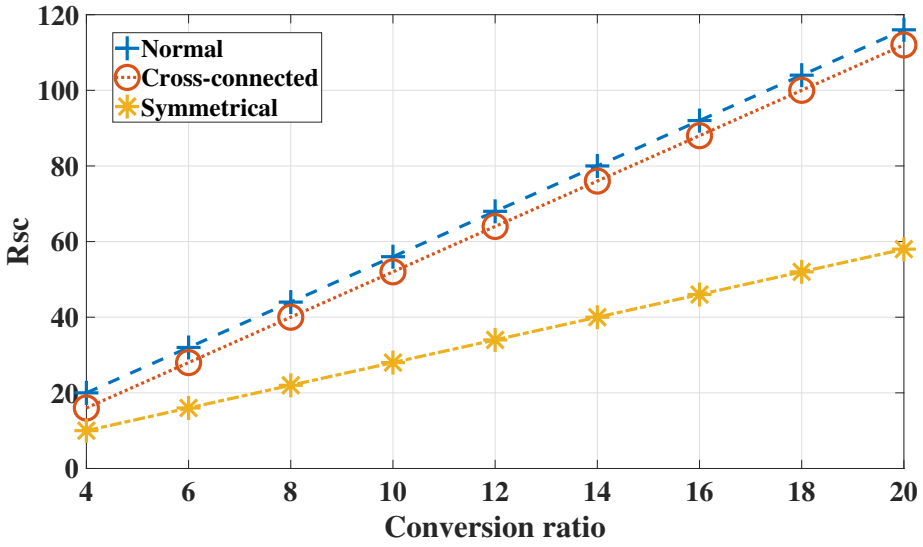


Figure 5.1: Comparison of R_{SC} of Dickson topologies.

5.1.3 Experiment

To confirm the feasibility of the cross-connected Dickson topology, the proposed topology was built on the bread board as shown in Figure 5.5. Figure 5.6 shows the circuit schematic for the proposed one. The experimental components are listed in Table 5.1. The switches (photo MOS relays) are connected to the Darlington

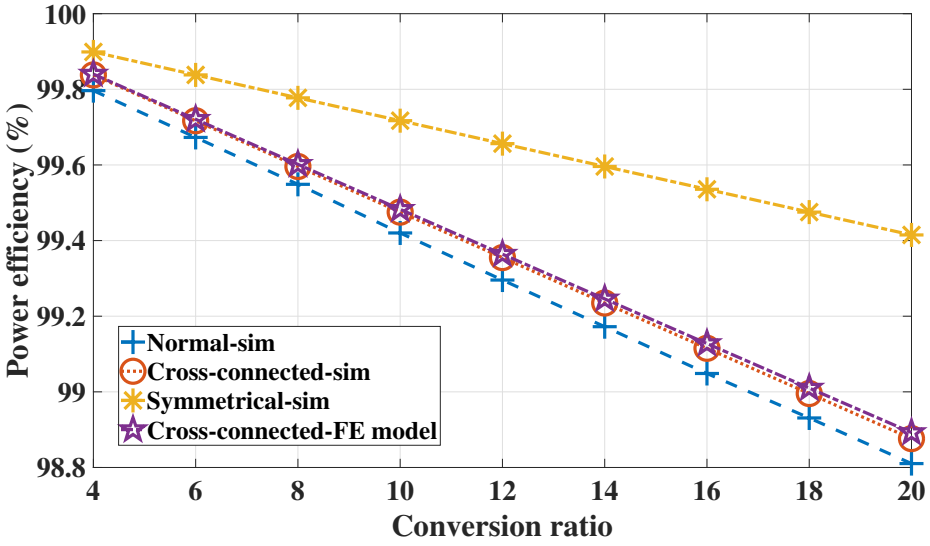


Figure 5.2: Comparison of power efficiencies of Dickson topologies.

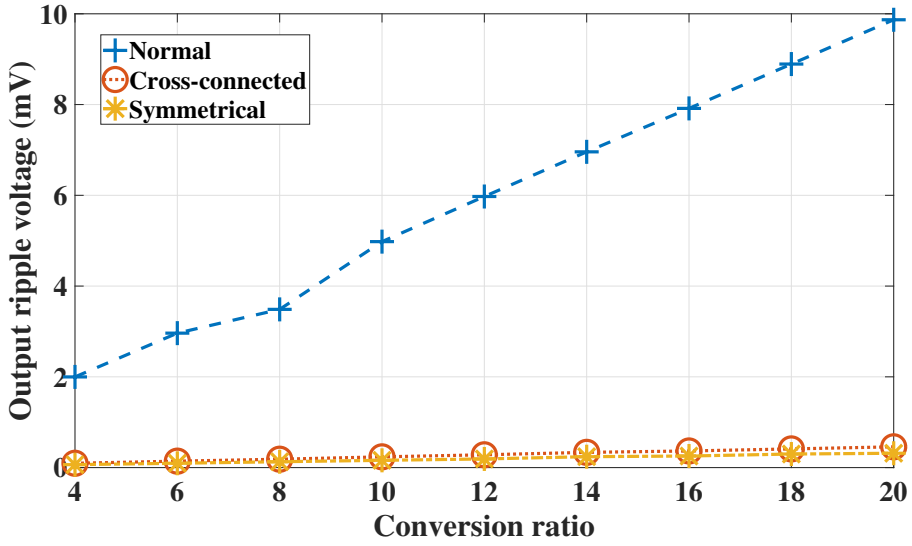
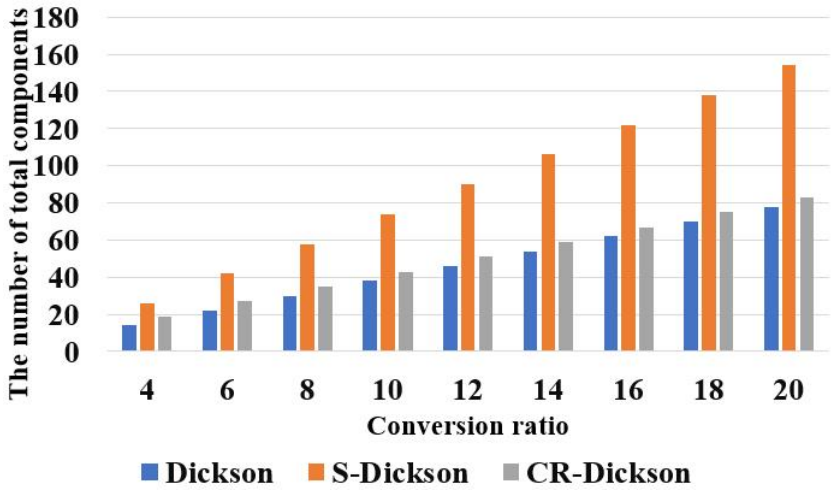
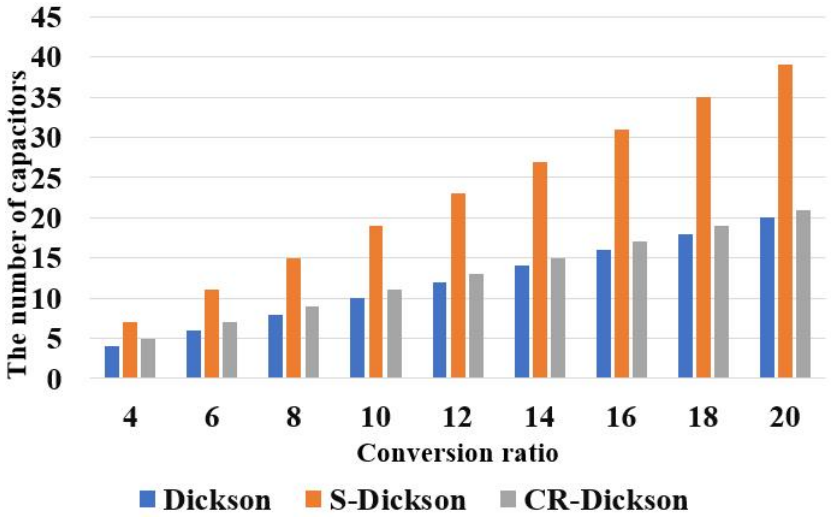


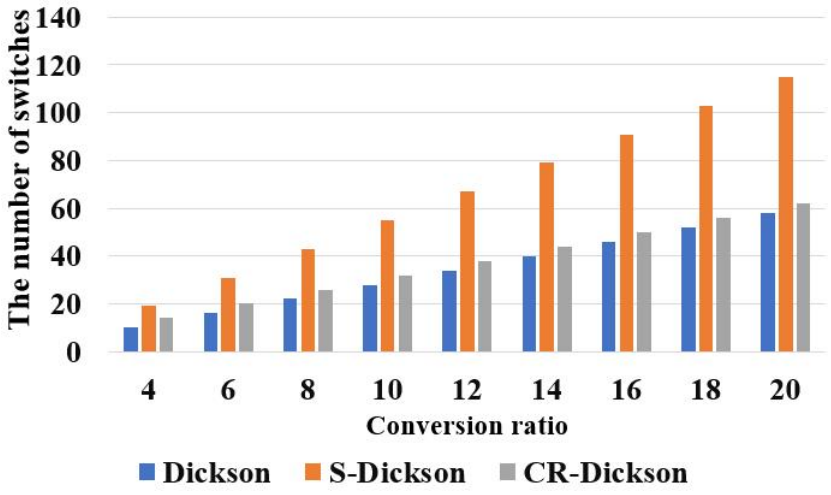
Figure 5.3: Comparison of output ripple voltages of Dickson topologies.



(a) The number of total components (Dickson topolgoies)



(b) The number of capacitors (Dickson topolgoies)



(c) The number of switches (Dickson topolgoies)

Figure 5.4: The number of circuit components of Dickson topologies

transistor arrays (TD6203APG) to drive the switches safely. The microcontroller (PIC12F629-I/P) inputs the control clock pulses into the Darlington transistor arrays.

The experiment setup is listed in Table 5.2. The measured output voltage is described in Figure 5.7. Comparing with the calculated output voltage (1.5979V) based on the FE model, the error is 0.0117V. The output voltage was measured by the oscilloscopes (MSOX2014A) with the bandwidth 100 Mhz and the ADC (analog to digital converter) bits of 8 bits [84].

Table 5.1: Circuit components of experimental circuit

Parts	Components	Specifications
Converter	Switch(On-resistor)	AQV212(0.83 Ω)
	Capacitor	33 μF
Control	Micro controller	PIC12F629-I/P
	Darlington transistor arrays	TD6203APG
	Current control resistance	330 Ω
Ouput load	Resistor	10 k Ω

Table 5.2: Experiment setup

Parameters	Values
Input voltage	400mV
Period of clock pulses	4ms
Duty ratio of clock pulses	50%

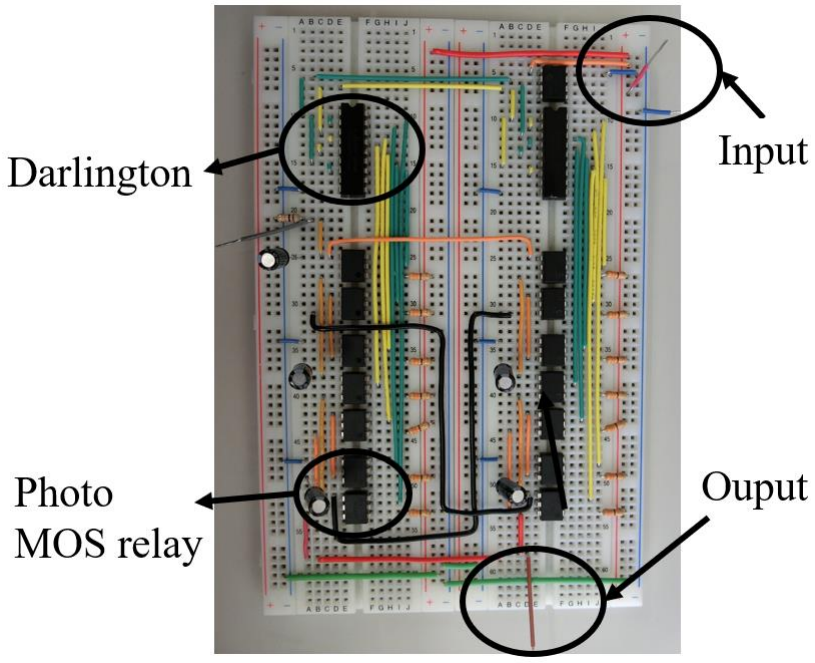


Figure 5.5: Experimental circuit of cross-connected Dickson topology.

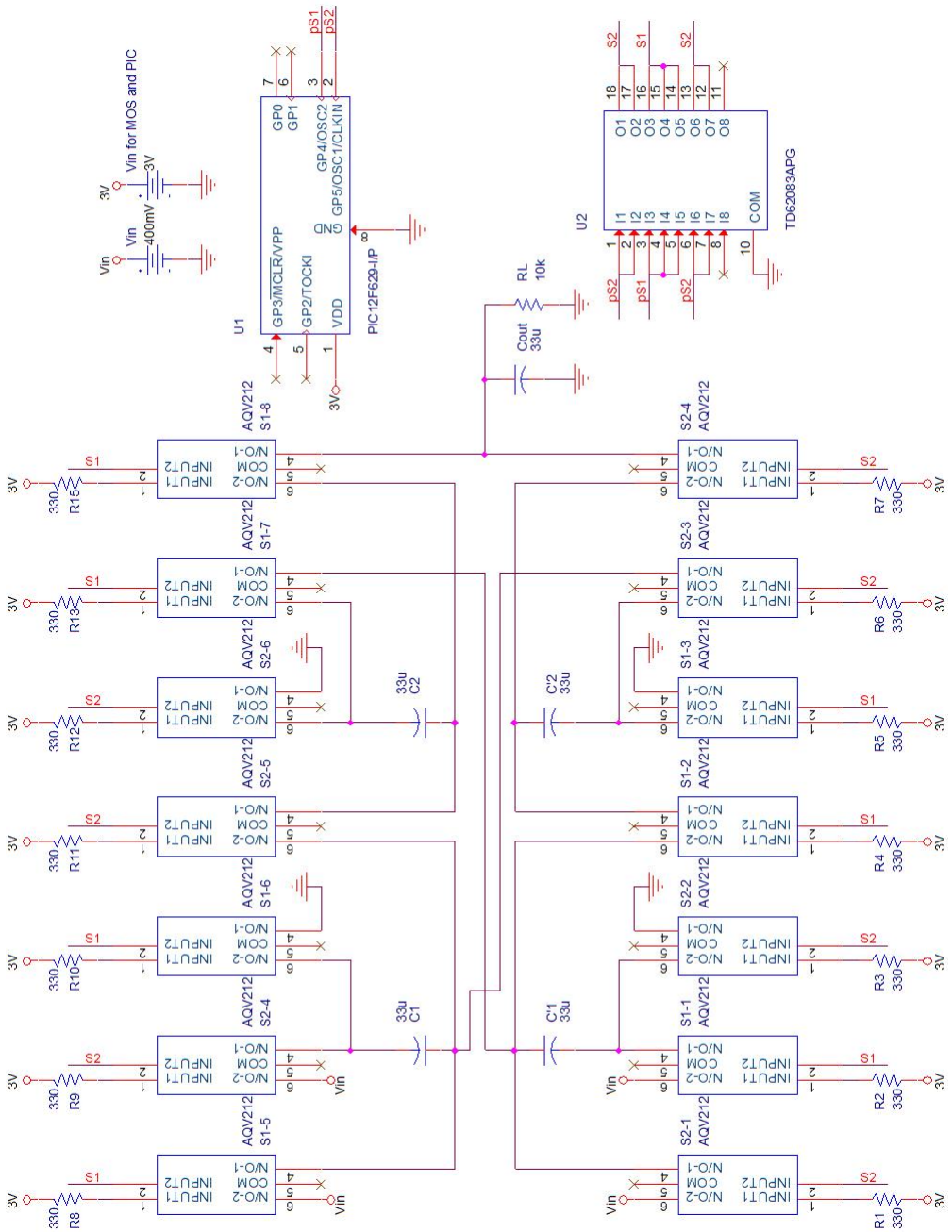


Figure 5.6: Experimental circuit schematic for cross-connected Dickson topology.

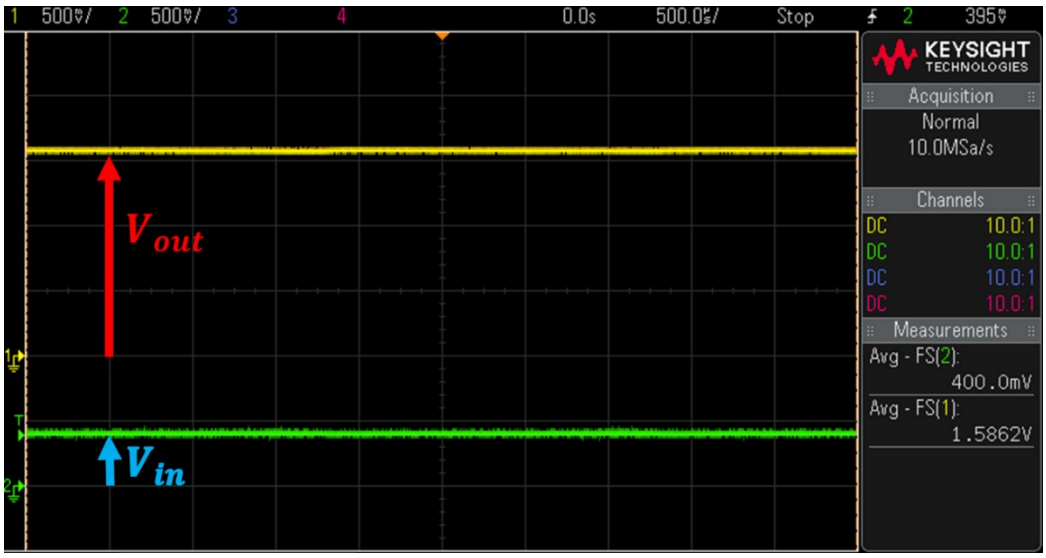


Figure 5.7: Measured output voltage of cross-connected Dickson topology.

5.2 Enhanced Cross-connected Fibonacci Topology

5.2.1 Theoretical Analysis

The proposed topology is analyzed by the FE model. In a steady state, the charge amounts of all capacitors satisfy the following equation according to the principle of capacitor amp-second balance and the symmetrical structure.

$$\begin{aligned} \Delta q_{T_1}^k + \Delta q_{T_2}^k &= 0, \\ \Delta k_{T_1}^k + \Delta k_{T_2}^k &= 0, \\ \Delta q_{T_1}^k = \Delta k_{T_2}^k &= -\Delta q_{T_2}^k = -\Delta k_{T_1}^k, \end{aligned} \tag{5.13}$$

where $(1 \leqq k \leqq n)$ and $\Delta q_{T_i}^k$ and $\Delta k_{T_i}^k$ is the k-th capacitor of the cell 1 and 2 in state-i $(i = 1, 2)$, respectively.

By setting the duty ratio D to 50%, T can be written as:

$$T = \sum_{i=1}^{2} T_i \quad \text{and} \quad T_1 = T_2 = \frac{T}{2}, \tag{5.14}$$

where $T_1 = (1 - D)T$ and $T_2 = DT$.

By using KCL, the relations of the electric charge amount of the input, output and capacitors at each operating state are calculated by:

$$\begin{aligned}
\text{State-1}: \Delta q_{T_1,V_{in}} &= \Delta q^1_{T_1} - \Delta k^1_{T_1} \\
\Delta k^1_{T_1} &= \Delta q^2_{T_1} - \Delta k^2_{T_1} \\
\Delta q^2_{T_1} &= -\Delta q^3_{T_1} + \Delta k^3_{T_1} \\
&\vdots \\
\Delta k^{n-1}_{T_1} &= -\Delta k^n_{T_1} + \Delta q^n_{T_1} \\
\Delta q_{T_1,V_{out}} &= \Delta q^n_{T_1} + \Delta q^{out}_{T_1} \\
\text{State-2}: \Delta q_{T_1,V_{in}} &= \Delta k^1_{T_2} - \Delta q^1_{T_2} \\
\Delta q^1_{T_2} &= \Delta k^2_{T_2} - \Delta q^2_{T_2} \\
\Delta k^2_{T_2} &= -\Delta k^3_{T_2} + \Delta q^3_{T_2} \\
&\vdots \\
\Delta q^{n-1}_{T_2} &= -\Delta q^n_{T_2} + \Delta k^n_{T_2} \\
\Delta q_{T_2,V_{out}} &= \Delta k^n_{T_2} + \Delta q^{out}_{T_2}.
\end{aligned} \tag{5.15}$$

Substituion of Eq.5.13 into Eq.5.15 leads to

$$\begin{aligned}
\Delta q_{V_{out}} &= \Delta q_{T_1,V_{out}} + \Delta q_{T_2,V_{out}} \\
&= 2\Delta q^n_{T_1} \\
\Delta k^1_{T_1} &= -2^{n-2}\Delta q_{V_{out}}, \\
\Delta k^{n-1}_{T_1} &= -2\Delta q^n_{T_1} \\
&= -\Delta q_{V_{out}}, \\
\Delta q_{V_{in}} &= 4\Delta q^n_{T_1} \\
&= 2^n \Delta q_{V_{out}}.
\end{aligned} \tag{5.16}$$

From Eqs. 5.13-5.16, the relation of the average input and output current is given by:

$$\langle I_{in} \rangle = -2^n \langle I_{out} \rangle , \tag{5.17}$$

From Eq. 5.17, the conversion ratio $m_{ECCFibo}$ is given by:

$$m_{ECCFibo} = 2^n. \tag{5.18}$$

The consumed energy by on-resistors of switches during each operating state is calculated as:

$$\begin{aligned}\text{State-1 }:W_{T_1} &= \frac{R_{on}}{T_1}\left\{3\left(\Delta q_{T1}^{1}\right)^2+3\left(\Delta q_{T1}^{2}\right)^2+3\left(\Delta q_{T1}^{3}\right)^2+3\left(\Delta q_{T1}^{4}\right)^2+\cdots\right. \\ &\quad \left.+4\left(\Delta q_{T1}^{n}\right)^2\right\} \\ &= \frac{2^{2n-2}R_{on}}{T_1}\left(\Delta q_{V_{out}}\right)^2 \\ \text{State-2 }:W_{T_2} &= W_{T_1}\end{aligned} \tag{5.19}$$

With the 50% duty ratio, the total consumed energy during one operating cycle is obtained as:

$$\begin{aligned}W_T &= \sum_{i=1}^{2} W_{T_i} = 2W_{T_1} = \frac{2^{2n-1}R_{on}}{T_1}\left(\Delta q_{T_{V_{out}}}\right)^2 \\ &= \frac{2^{2n}R_{on}}{T}\left(\Delta q_{T_{V_{out}}}\right)^2.\end{aligned} \tag{5.20}$$

Comparing Eqs. 5.20 and 2.14, the R_{SC} of the enhanced cross-connected Fibonacci topology is given by:

$$R_{SC} = 2^{2n}R_{on}. \tag{5.21}$$

The K-matrix of the proposed topology can be expressed by:

$$\begin{bmatrix}\langle V_{in}\rangle \\ \langle I_{in}\rangle\end{bmatrix} = \begin{bmatrix}1 & 0 \\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 2^{2n}R_{on} \\ 0 & 1\end{bmatrix}\begin{bmatrix}\langle V_{out}\rangle \\ -\langle I_{out}\rangle\end{bmatrix}. \tag{5.22}$$

From above steps, the maximum efficiency and output voltage of the enhanced cross-connected Fibonacci topology is calculated as:

$$\eta_{max} = \frac{R_L}{R_L + R_{SC}} = \frac{R_L}{R_L + 2^{2n}R_{on}} \tag{5.23}$$

$$V_{out\_max} = \frac{R_L}{R_L + 2^{2n}R_{on}}V_{in}. \tag{5.24}$$

Although the n is assumed to be an even number in this analysis, the result of R_{SC} is the same at both of the even and odd number cases.

5.2.2 Simulation and Comparison

The suggested topology was simulated with the conditions as listed in Table 3.9. There are trivial errors between the calculated and simulated power efficiency at different conversion ratios as shown in Figure 5.8.

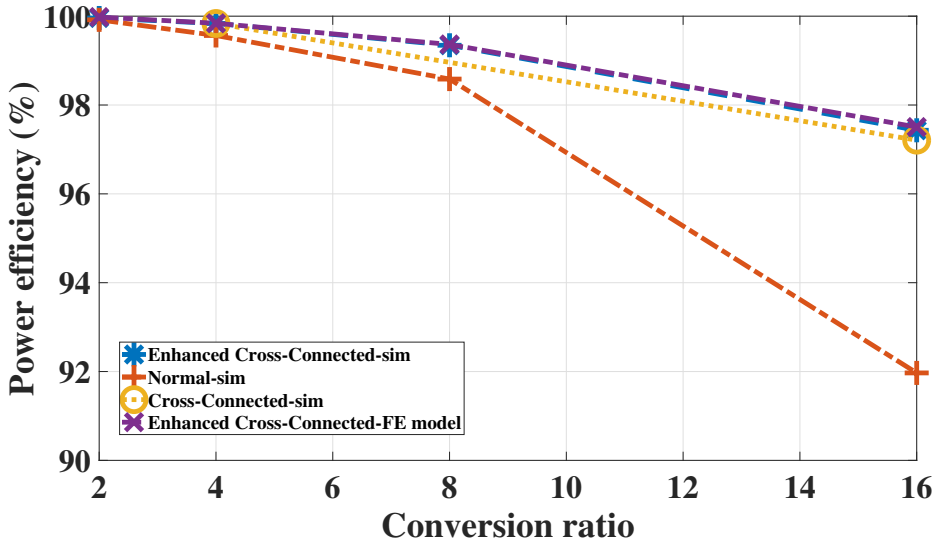


Figure 5.8: Comparison of power efficiencies of enhanced cross-connected Fibonacci topology.

The R_{SC} of the proposed topology is the lowest among three Fibonacci topologies, by which the proposed one has the highest power efficiency among them as depicted in Figure 5.9. By the benefit of the symmetric structure, the output ripple voltage of the proposed topology is lower than the normal one at all conversion ratios as shown in 5.10.

Figure 5.11 describes the number of required circuit components for three Fibonacci topologies. Comparing with the normal Fibonacci topology, the circuit size of the proposed one is bigger than that of the normal one. However, the proposed one can improve the power efficiency. In the comparison with the cross-connected topology, the proposed one can generate the more various kinds of output voltage with higher power efficiency. Moreover, the proposed one is required to have the smaller number of circuit components at the conversion ratio of 16.

When an SC DC-DC topology demands the small number of circuit components, low output ripple voltage and high level step-up gain, the enhanced cross-connected topology can fit in the requirements.

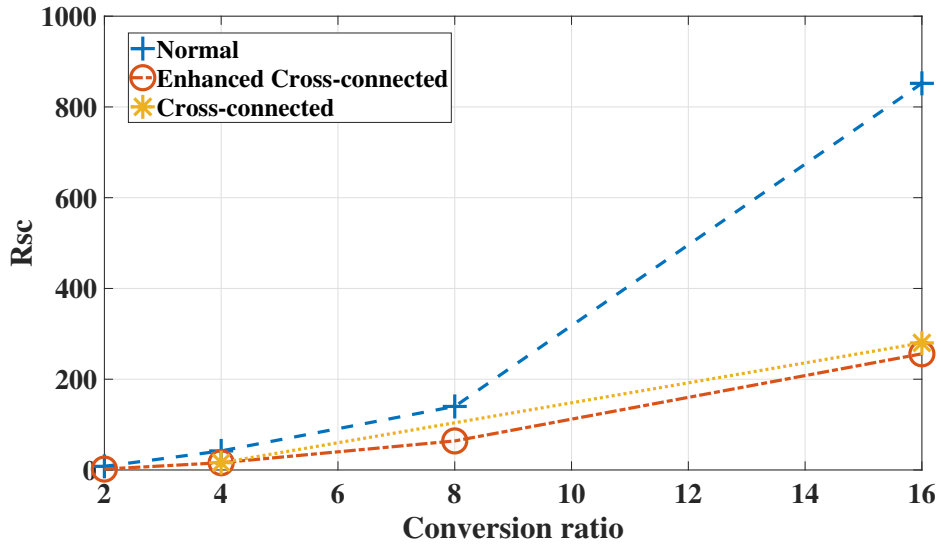


Figure 5.9: Comparison of R_{SC} of enhanced cross-connected Fibonacci topology.

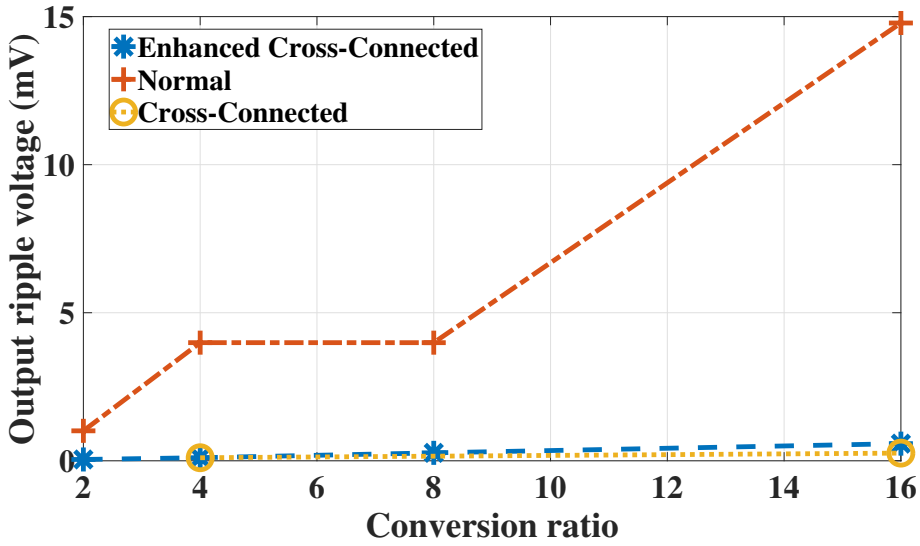
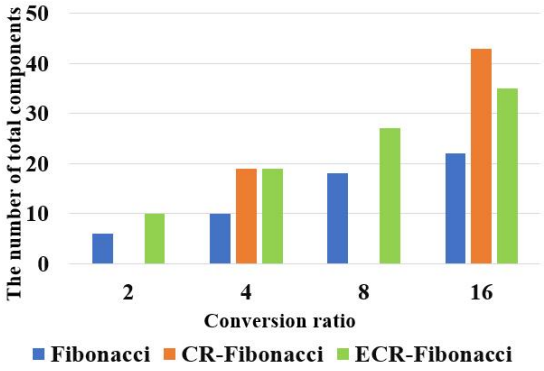


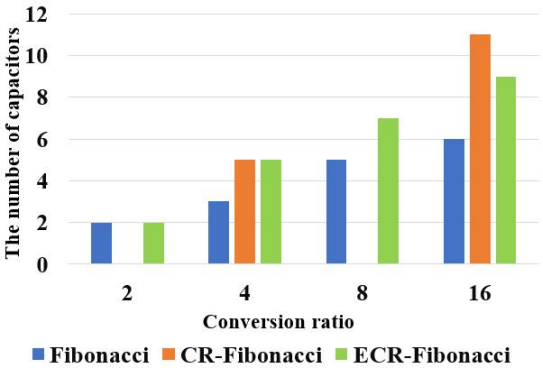
Figure 5.10: Comparison of output ripple voltages of enhanced cross-connected Fibonacci topology.

5.2.3 Experiment

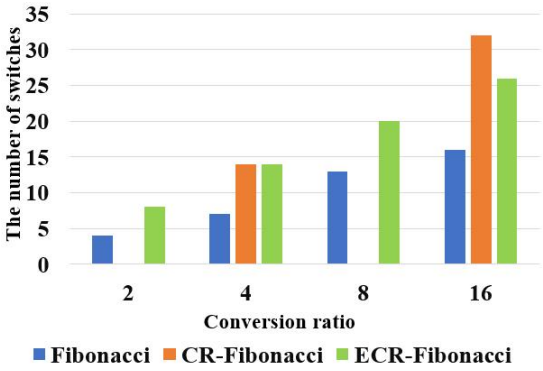
To confirm the feasibility of the enhanced cross-connected Fibonacci topology, it was built on the breadboard as shown in Figure 5.12(a). Additionally, the normal Fibonacci topology was also constructed on the breadboard to compare the performance of the proposed topology as described in Figure 5.12(b). Figure 5.13



(a) The number of total components (Fibonacci topolgoies)



(b) The number of capacitors (Fibonacci topolgoies)



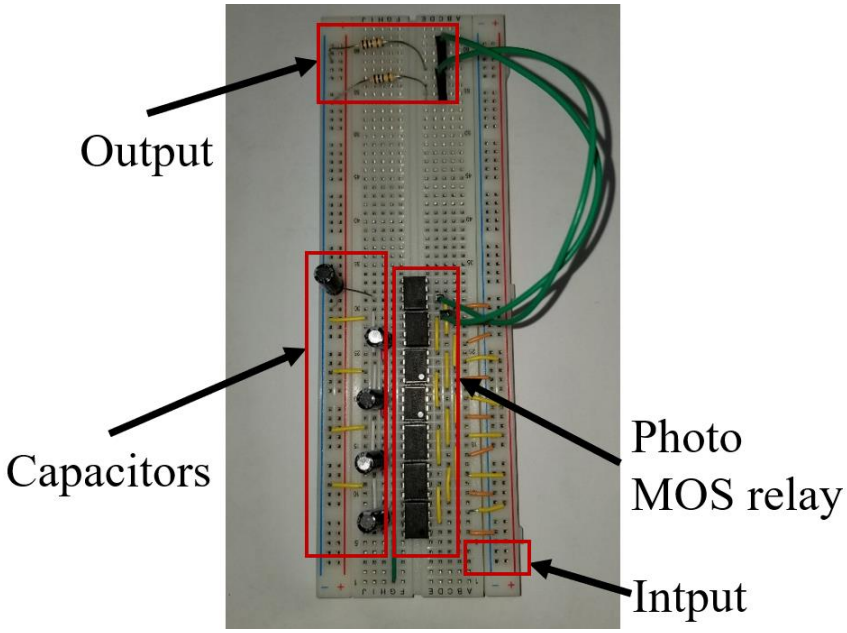
(c) The number of switches (Fibonacci topolgoies)

Figure 5.11: The number of circuit components of Fibonacci topologies

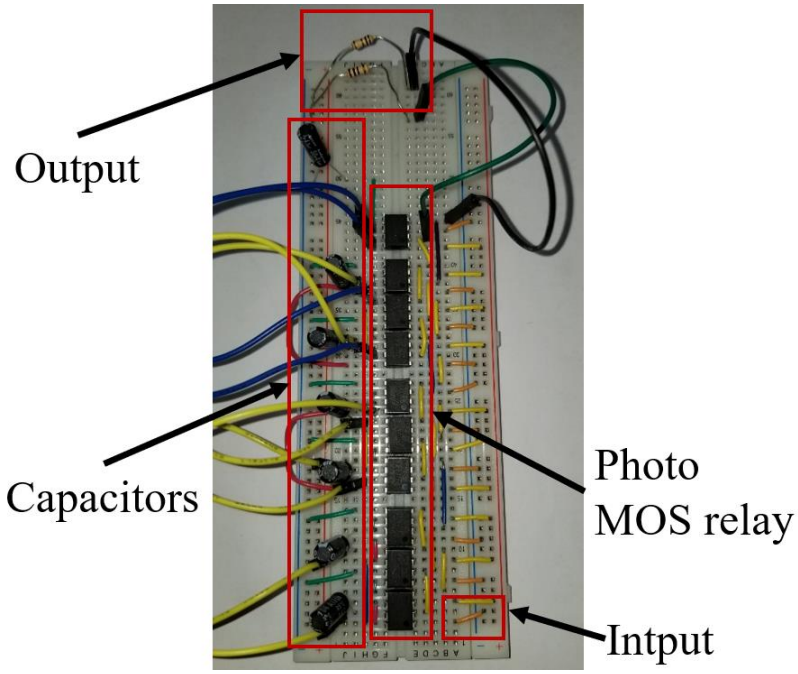
and Figure 5.14 show the circuit schematics for the normal and proposed ones, respectively. Table 5.3 lists the specifications of the used circuit components on two circuits. The experiment was performed with the condition as reported in Table 5.4.

As the output voltages measured by the oscilloscopes (MSOX2014A) are 3.05V and 2.83V, the step-up gains are 7.625 and 7.075, respectively. The measured output voltages of the normal Fibonacci topology are 2.96V and 2.68V, by which the step-up gains are 7.4 and 6.7, respectively. With this result, it is confirmed that the proposed one improves the output performance, comparing with the normal one.

Comparing the output voltage waveforms of two topologies, the output ripple of the normal Fibonacci topology is higher than that of the proposed one.



(a) Normal Fibonacci topology



(b) Enhanced cross-connected Fibonacci topology

Figure 5.12: Fibonacci topologies on breadboard.

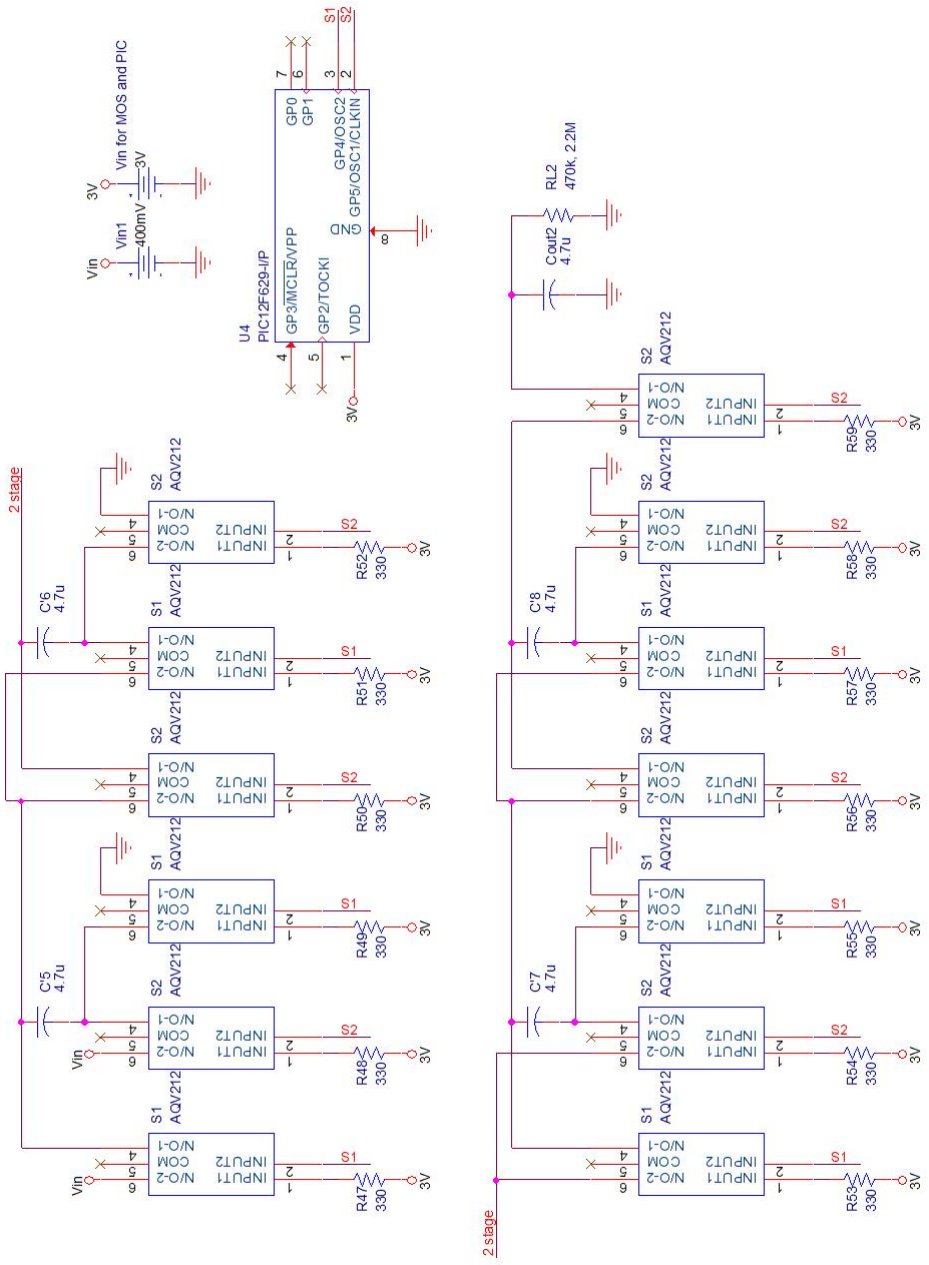


Figure 5.13: Experimental circuit schematic for normal Fibonacci topology.

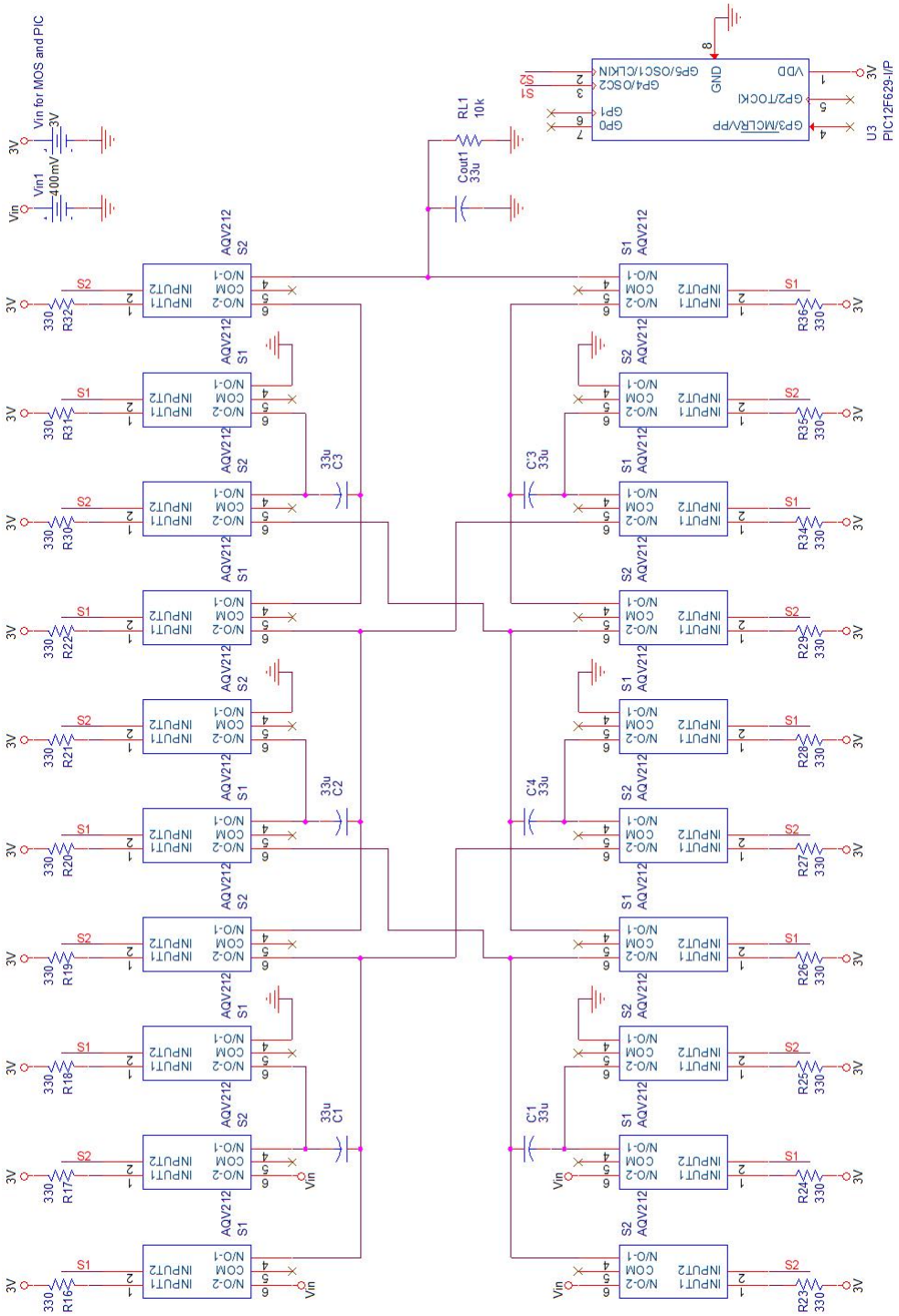
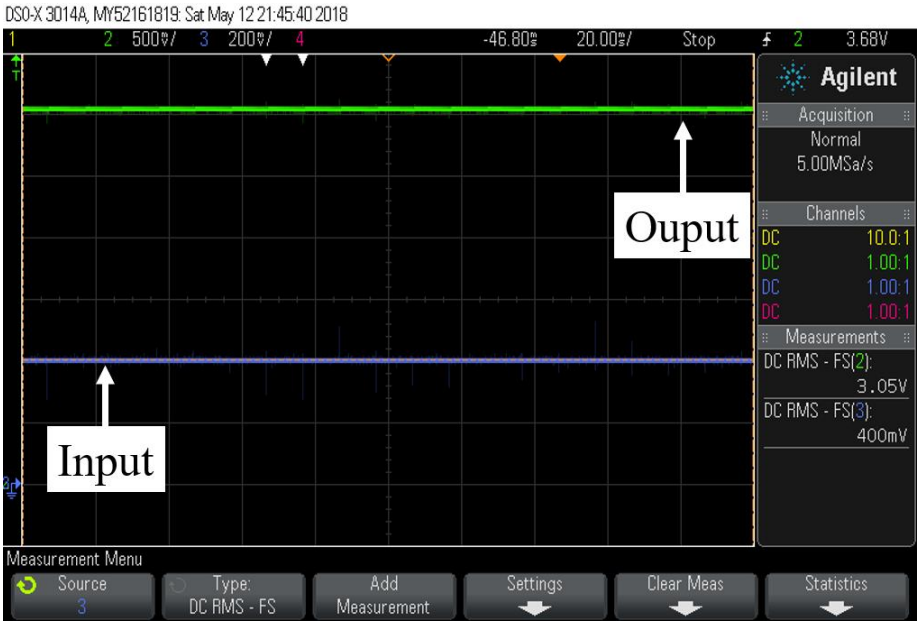
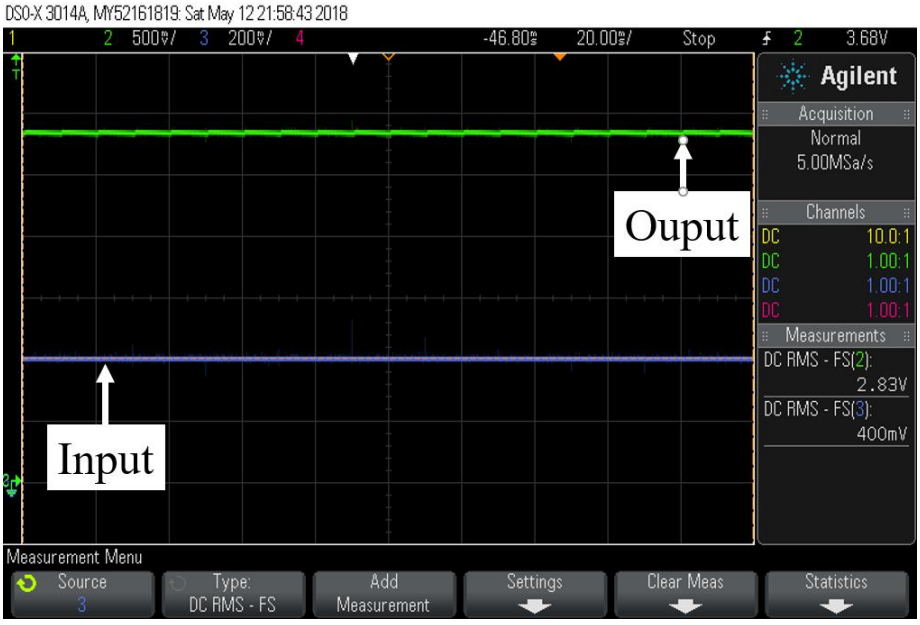


Figure 5.14: Experimental circuit schematic for enhanced cross-connected Fibonacci topology.

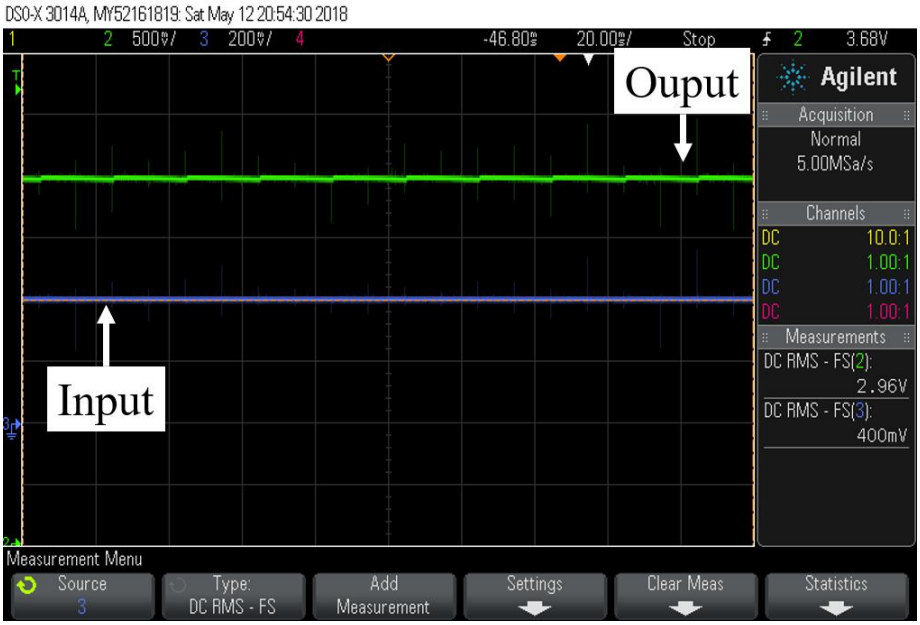


(a) 2.2MΩ

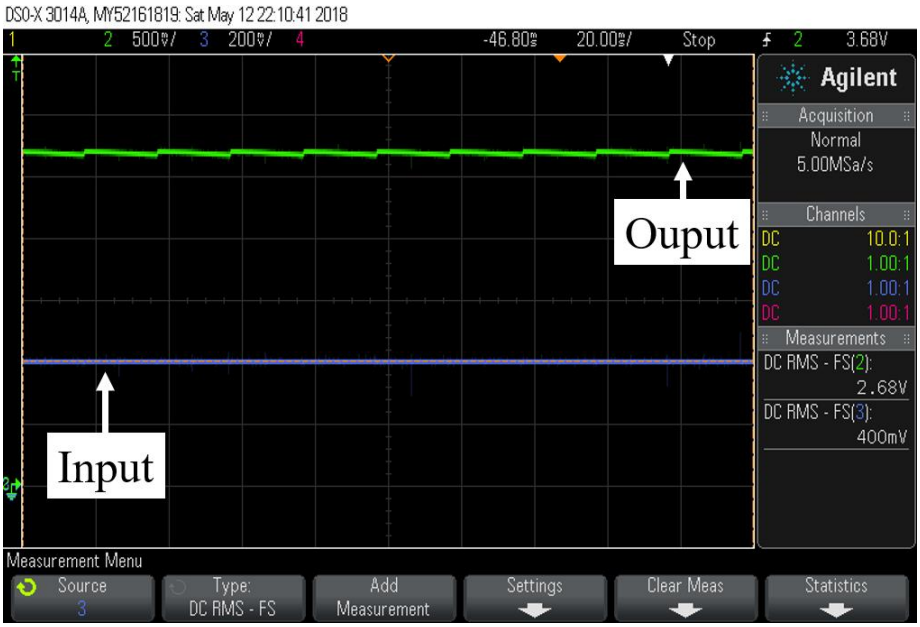


(b) 470kΩ

Figure 5.15: Measured output voltage of enhanced cross-connected Fibonacci topology.



(a) 2.2MΩ



(b) 470kΩ

Figure 5.16: Measured output voltage of normal Fibonacci topology.

Table 5.3: Circuit components of experimental circuit for Fibonacci topologies

Parts	Components	Specifications
Converter	Switch(On-resistor)	AQV217(20 Ω)
	Capacitor	$4.7\mu F$
Control	Micro controller	PIC12F629-I/P
Ouput load	Resistor	470 k Ω, 2.2MΩ

Table 5.4: Experiment setup for Fibonacci topologies

Parameters	Values
Input voltage	400mV
Period of clock pulses	20ms
Duty ratio of clock pulses	50%

Chapter 6

Conclusion and Future Works

6.1 Conclusions

In this thesis, we have suggested two new switched capacitor (SC) DC-DC converter topologies. SC DC-DC converters are suitable for mobile products including energy harvest systems because the lack of magnetic components prevent EMC (electromagnetic compatibility) or EMI (electromagnetic interference) problems and make their circuit size small, comparing with inductor-based converters.

In Chapter 2, a trivial SC DC-DC converter with the conversion ratio of 1 in a steady state was analyzed to derive its gain function. From the variations of the gain function by varying each parameter, it is confirmed that the on-resistor of the switch and output load are the dominant parameters to have influence on the gain. For this reason, the four-terminal equivalent circuit model or FE model is selected because in the model, the resistance parameter R_{SC} and R_L are the only ones to affect the output performance of the modeled converter.

In Chapter 3, we suggest a way to categorize SC DC-DC converter topologies according to the number of outermost mesh including their input and output ports. By this way, the converter topologies were sorted in two groups of core and modified topologies. The converter topologies were analyzed based on the FE model. Then, they were simulated to measure the power efficiencies and output ripple voltages. With these calculated and simulated data, the topologies were compared at different conversion ratios from 2 to 20:

- Comparison of core topologies (Dickson, series-parallel and Fibonacci).

- Comparison of modified topologies according to each topology family (SCVM, symmetrical Dickson and cross-connected Fibonacci).

Among core topologies, the highest power efficient topology is the Dickson topology and the Fibonacci topology has the worst power efficiency over the conversion ratio of 13. From this comparison, it is confirmed that three operating states mode can cause higher output ripple voltages. The topology of the smallest circuit size is the Fibonacci topology.

From the comparison of the modified topologies, the pros and cons of three modifying ways are derived:

- Cascaded structure: Although the modified topology has limited conversion ratio, this way can reduce the number of circuit components.

- Symmetric structure: the symmetrical construction can improve power efficiency and dramatically reduce output ripple voltages (maximum 30 times at the case of symmetrical Dickson topology). The increase of circuit components is a flaw.

- Cross-connected structure: This modifying way can improve power efficiencies and output ripple voltages. However, the circuit size becomes bigger.

In Chapter 4 and 5, we suggested the cross-connected Dickson topology and enhanced cross-connected Fibonacci topology. The new Dickson topology improved its power efficiency and output ripple voltage, comparing to the normal Dickson topology. However, there was room for reducing circuit size and improving conversion ratio if two topologies consist of the similar number of circuit components. In this regard, the new Fibonacci topology was suggested. The power efficiency of the new Fibonacci topology was the highest among different Fibonacci topologies. Also, the output ripple voltage was reduced. The feasibilities of both new topologies were verified by building them on the breadboard.

Throughout this research, SC DC-DC converter topologies have been categorized and analyzed. The result of Chapter 3 can help future designers or researchers make a better selection of an SC DC-DC converter topology. The works of chapter 4 and 5 built a basis of efficiency energy harvesting systems.

6.2 Future Works

In this works, the SC DC-DC converter topologies were analyzed in a steady state. Therefore, we need the analysis of the converters in a transient state. This will be performed based on the FE model. In the FE model, we fixed the duty ratio as 50% or 1/3. By changing these ratios as $D1$ and $D2$ ($D1$, $D2$ and $D3$ at three operating states modes) and add minute variations (AC values) $d1$, $d2$ ($d1$, $d2$ and $d3$), the R_{SC} and output voltage can be derived. With calculating them, we will perform an AC analysis of the proposed topologies, which leads to its transient analysis and designing its controller.

When the controller is designed, we will compare classical controller (linear) such as PI, PID etc. with non-linear controller such as a controller based on the Fuzzy theory. Then, we will design our own controller for the proposed topologies.

Next, the prototype of the proposed topologies will be designed by discrete components on a PCB (printed circuit board). Using them, we will apply the proposed topologies to energy harvesting systems that treat with relatively higher power. For low or ultra-low power, the IC implementation of the proposed topology will be carried out.

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